Welcome To

ISSCC 2014
SESSION 20
Wireless Systems

A 40nm CMOS Receiver for 60GHz Discrete-Carrier Indoor Localization Achieving mm-Precision at 4m Range

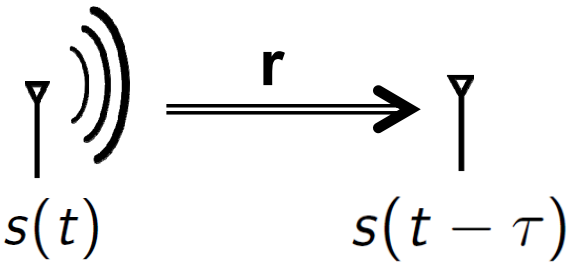
T. Redant, T. Ayhan, N. De Clercq, M. Verhelst, P. Reynaert, W. Dehaene

KU Leuven, ESAT-MICAS, Belgium

Outline

- Motivation
- System overview
- Range estimation algorithm
- IC implementation
- Measurements
- Conclusions

Motivation

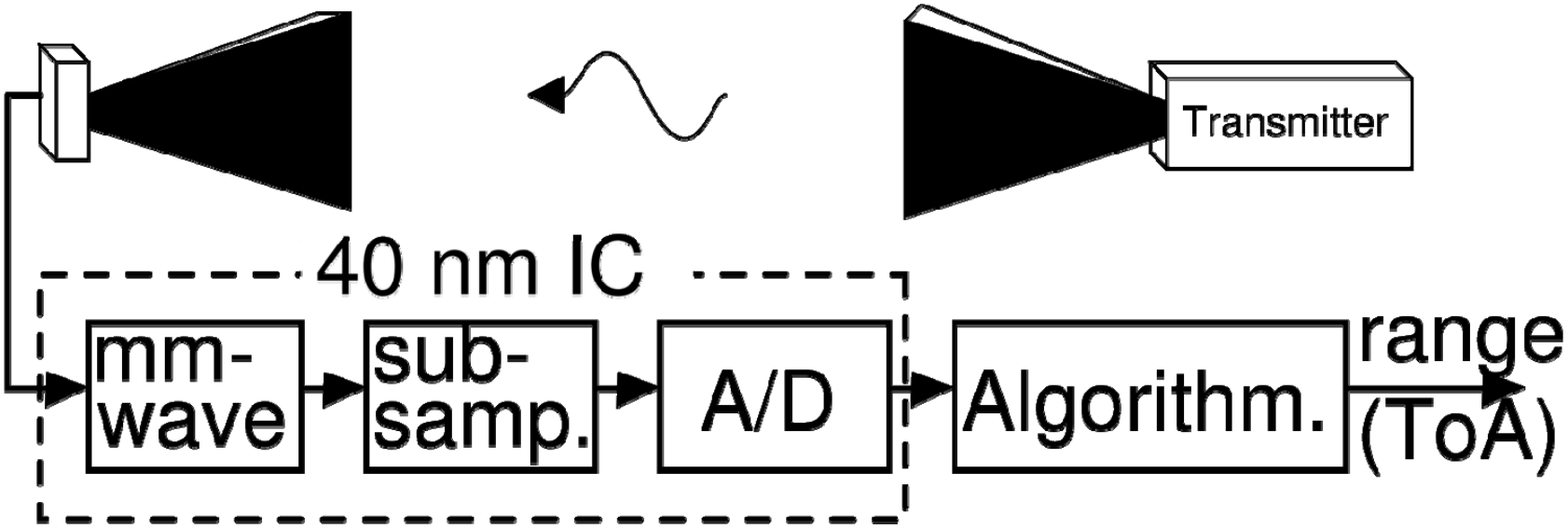


$$\mathrm{Var}_{\hat{r}} \geq \frac{c_{air}^{\,2} \cdot 3}{4 \cdot \pi^2 \cdot T \cdot \mathrm{SNR} \cdot \left[(f_c + BW/2)^3 - (f_c - BW/2)^3 \right]}$$

- G**BW** ~ g_m/C ~ P
- Solution for low BW?
  - Obtaining a highly-precise range estimate
  - Ensuring high update speeds
- …Discrete spectrum…
- …A sub-Nyquist sampling technique…

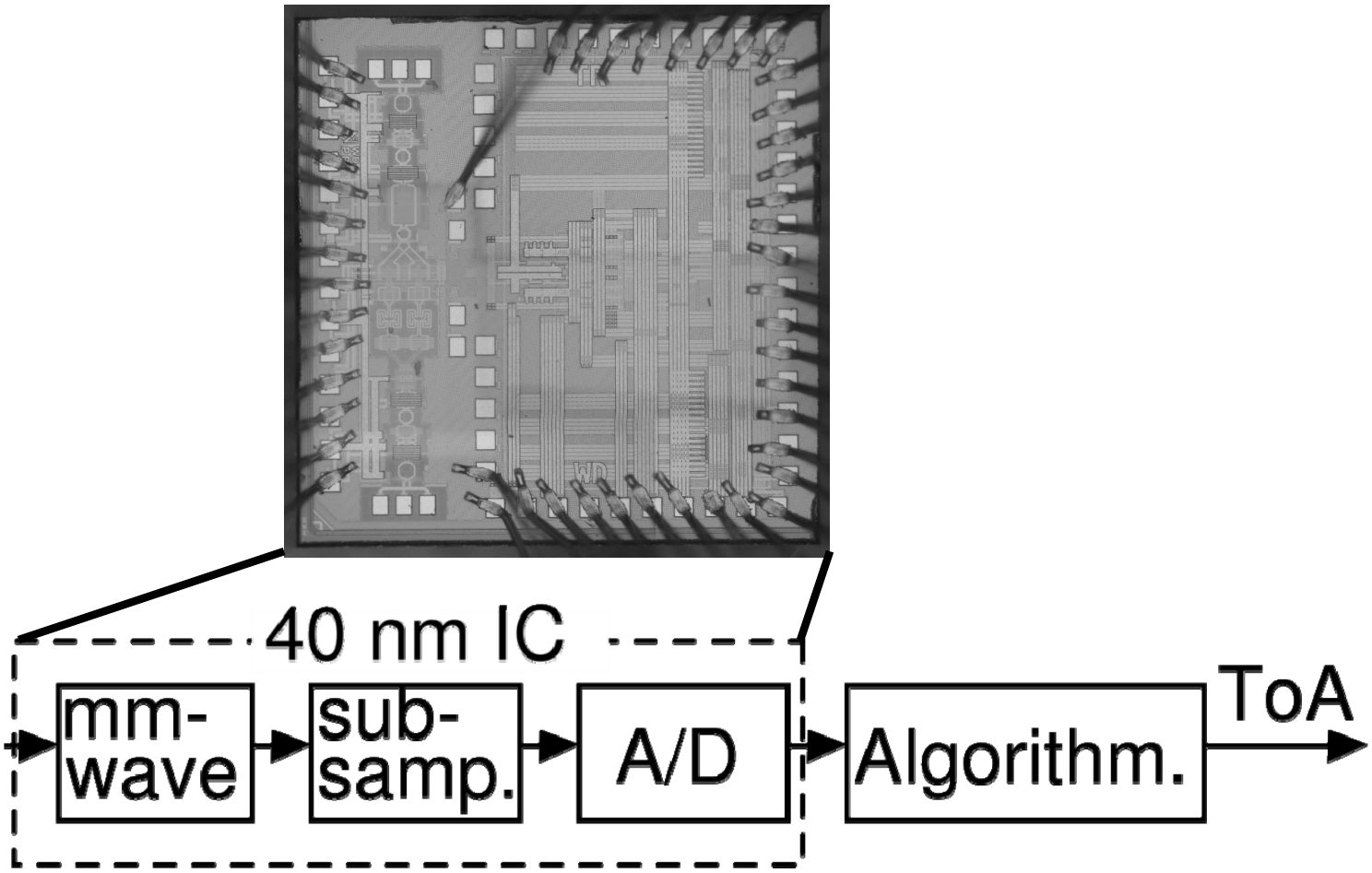
Motivation

- Custom & joint approach
  - mm-wave circuits → high absolute BW
  - A/D topology → low BW
  - Algorithm



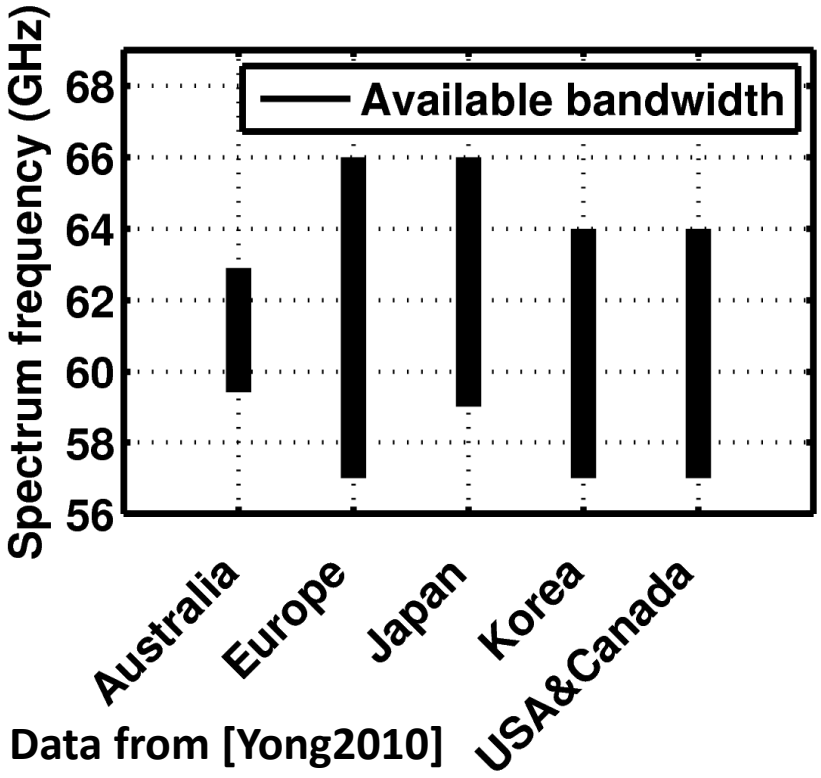
System overview - IC

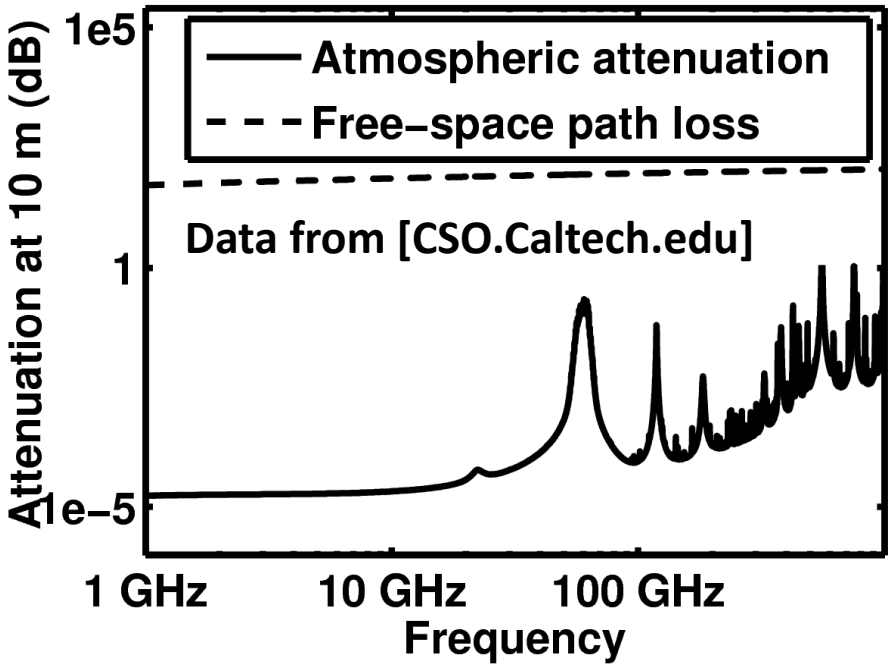
- Receiver IC



System overview – frequency

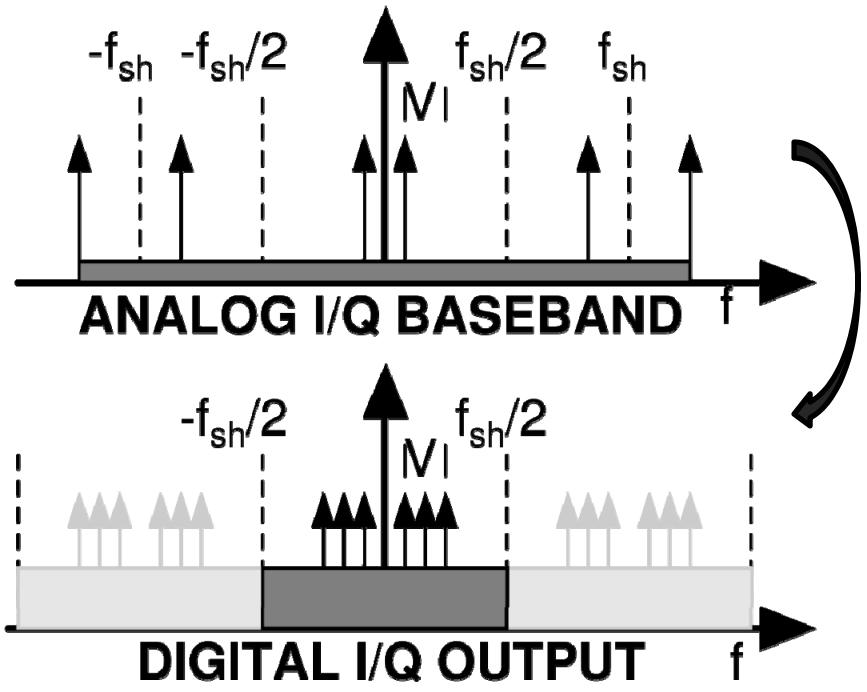
- 60 GHz band

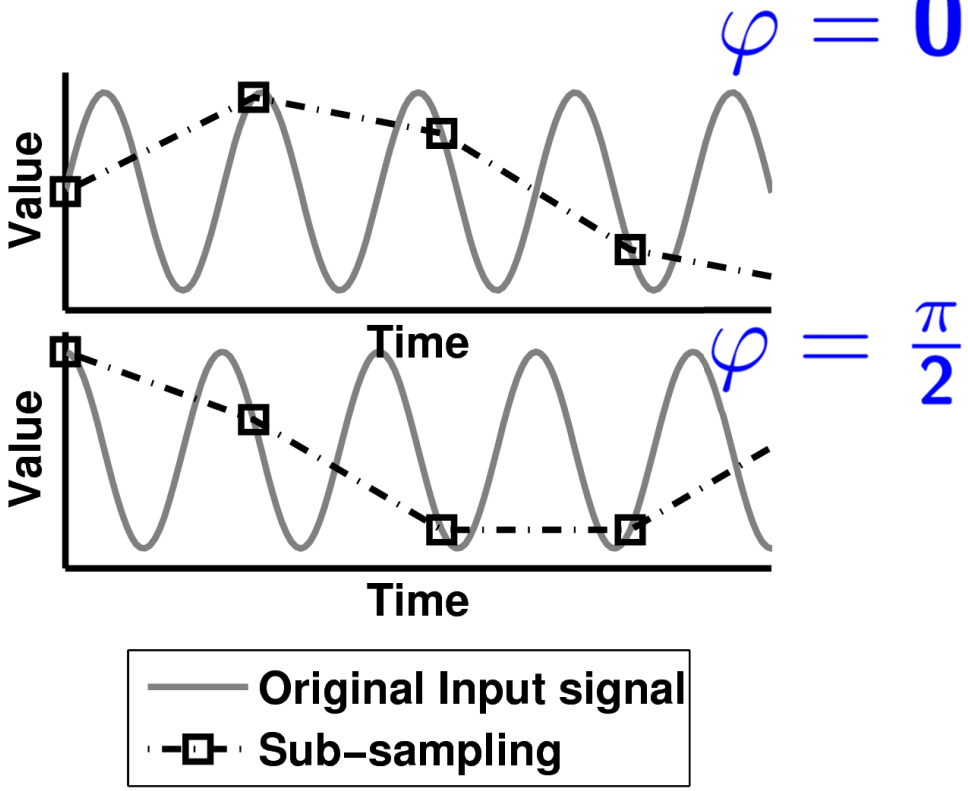




System overview – Main Concept

- **Use discrete spectrum signal**
  → aliasing-free sub-sampling & ranging?

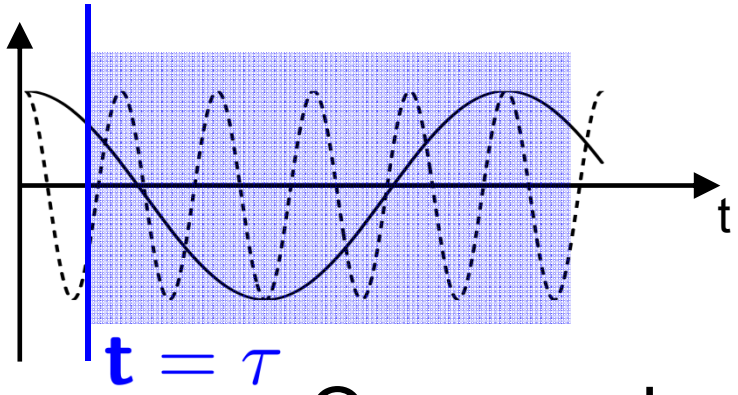


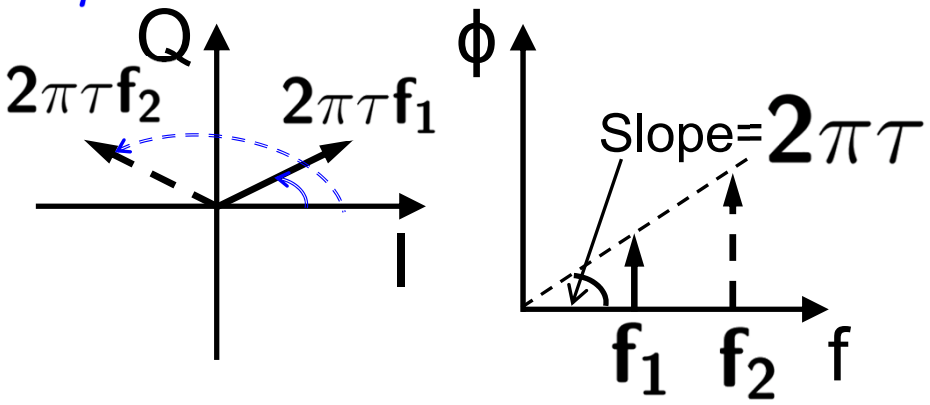


Algorithm (principle)

- Algorithm analyzes phases

$$\cos\left(2\pi f_c(t-\tau)\right)\cdot\sum_{i=-N/2}^{N/2-1} S_i\cdot e^{j\cdot 2\pi f_i\cdot(t-\tau)}$$





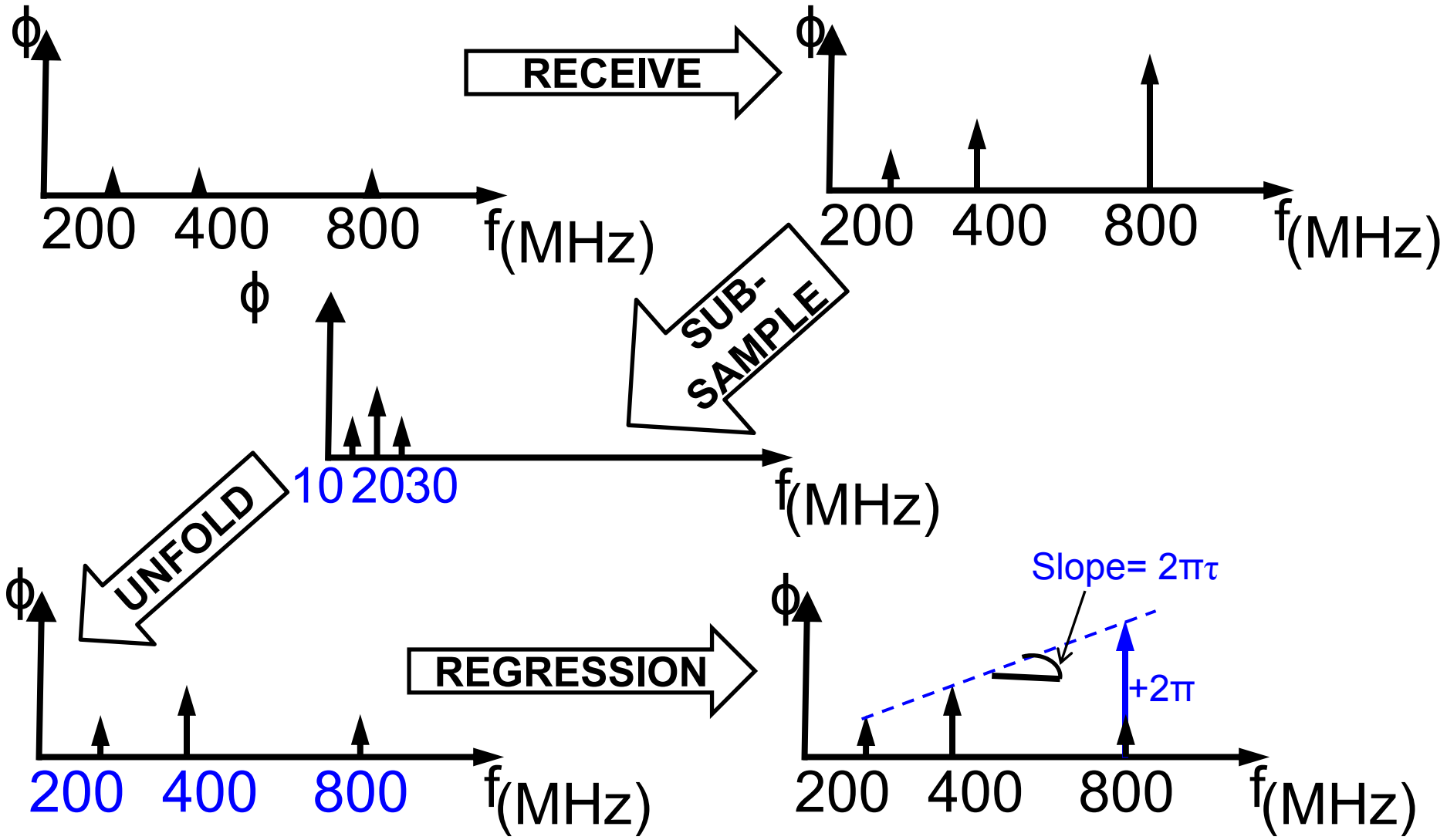
- Phase of carrier i:

$$\varphi_i = 2\pi\tau f_i$$

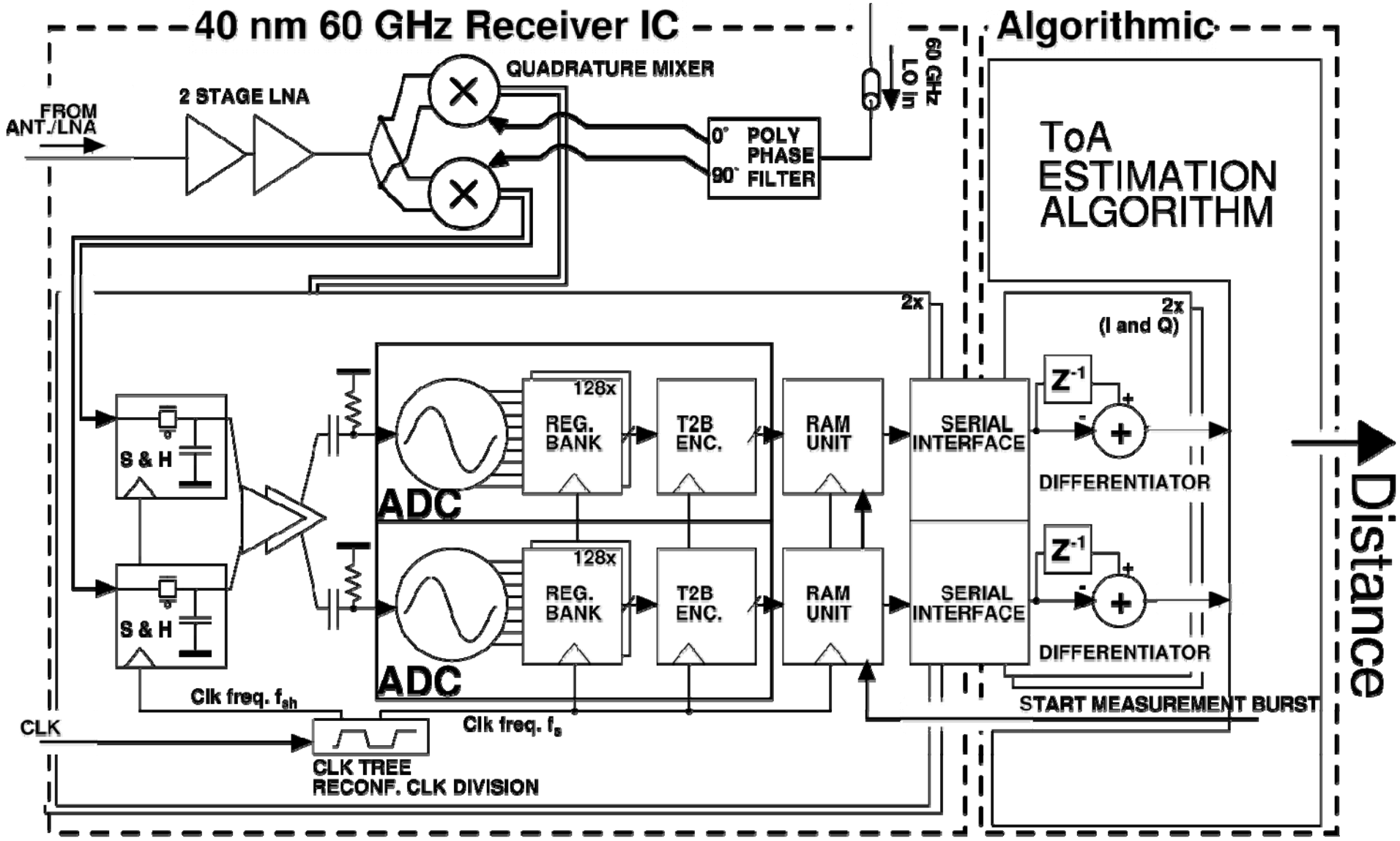
Slope ~ range

Algorithm

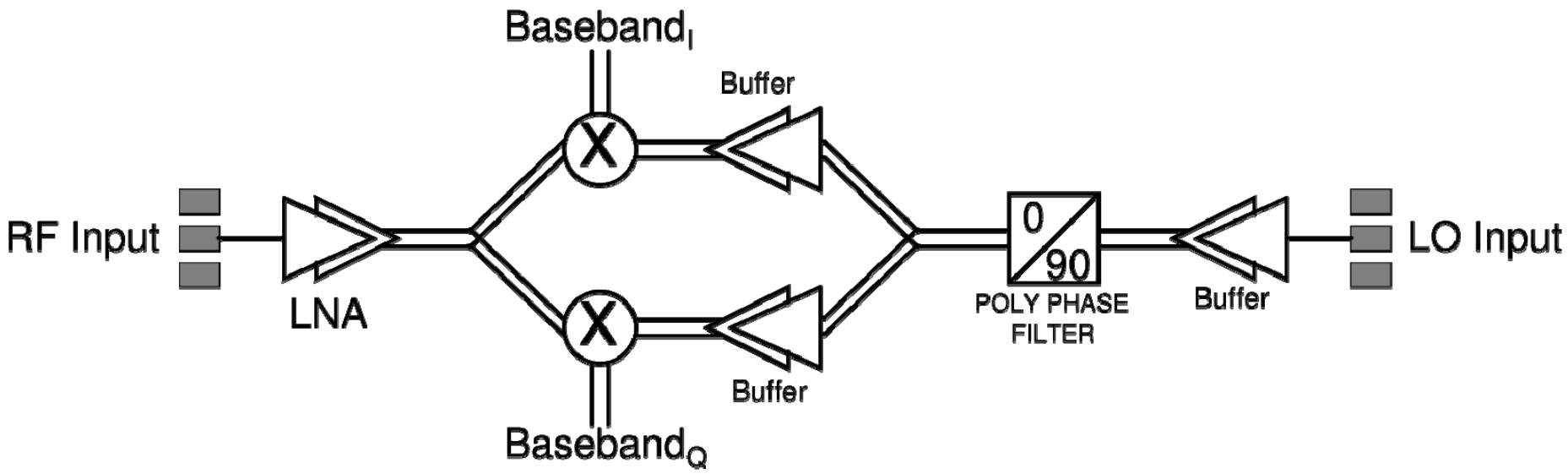
- Algorithm processes baseband signal



System implementation

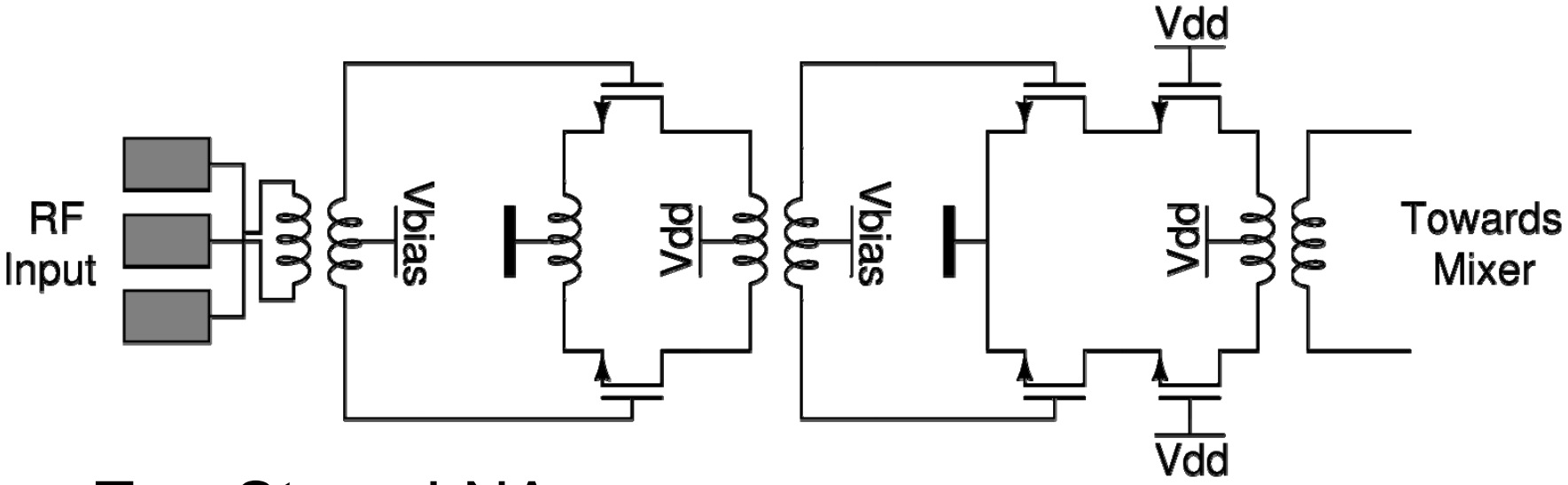


RF front-end



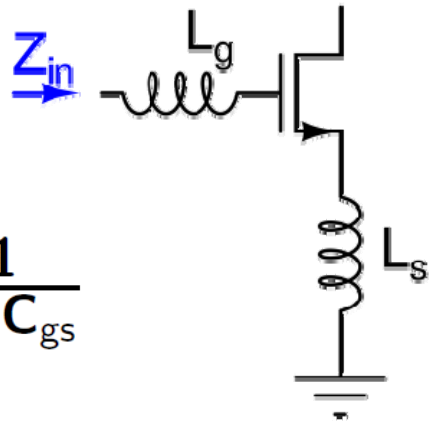
- Fully Differential
  - LNA + IQ Direct-Down conversion
  - IQ LO generation: Poly Phase Filter (PPF)
- Wideband impedance match
  - Transformer coupled stages
  - Slow Wave Transmission Lines (SWTL)

RF front-end (LNA)



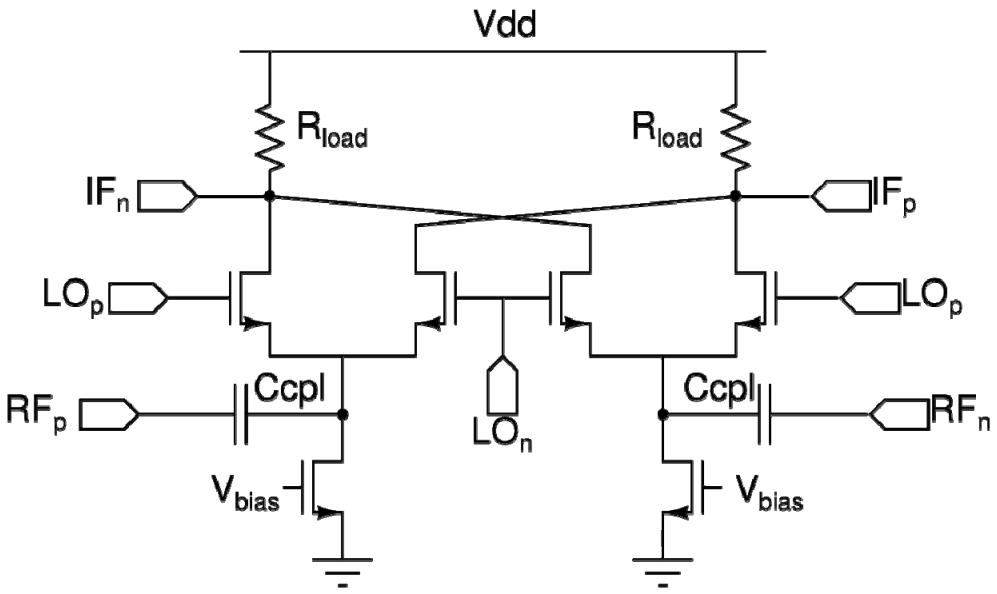
- Two Stage LNA
  - Inductive source degeneration
    - Easier to match

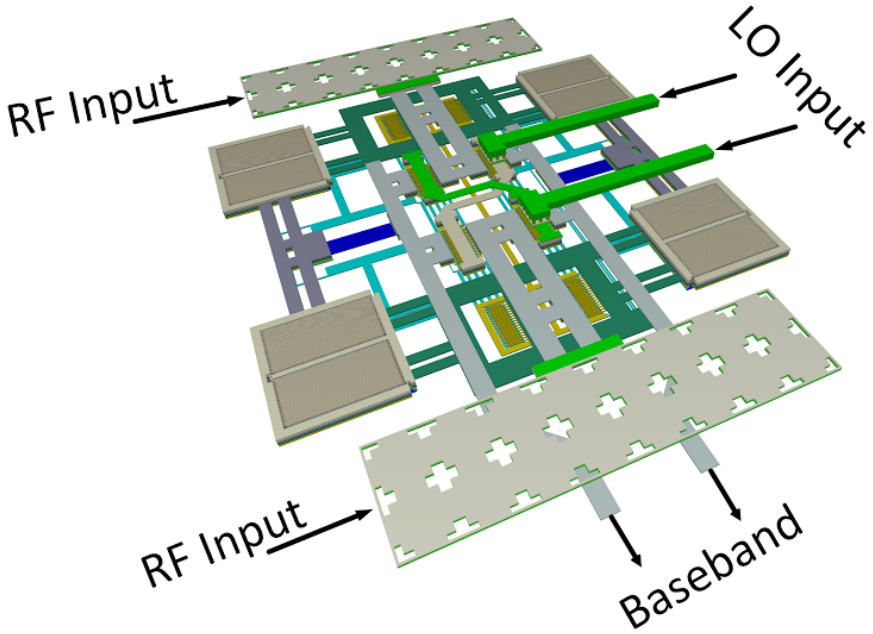
$$Z_{in} = \frac{L_s \cdot g_m}{C_{gs}} + j\omega \cdot (L_g + L_s) + \frac{1}{j\omega \cdot C_{gs}}$$



  - Cascode for extra gain

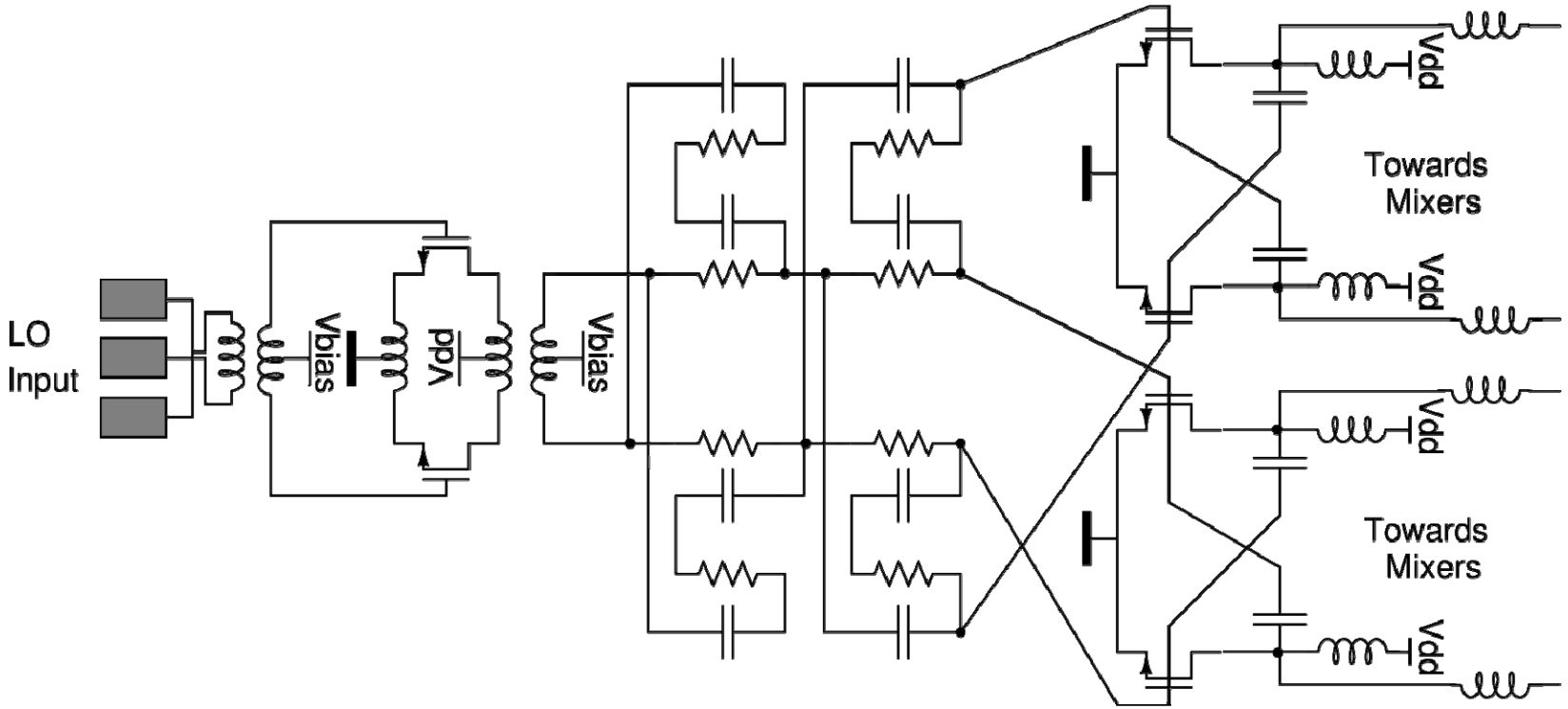
RF front-end (Mixer)





- Double Balanced Mixer
- Low V_{dd} → no transconductance stage
- RF signal → series coupling capacitors

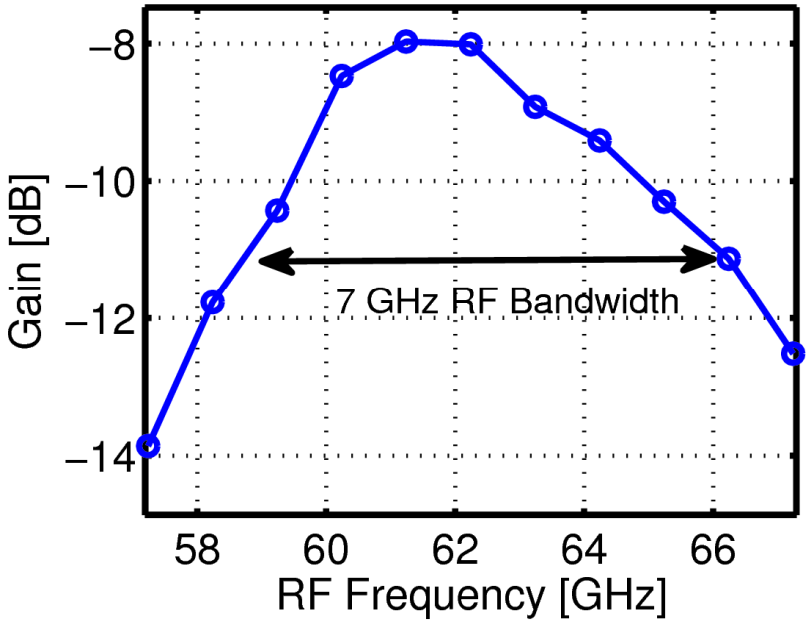
RF front-end (LO generation)

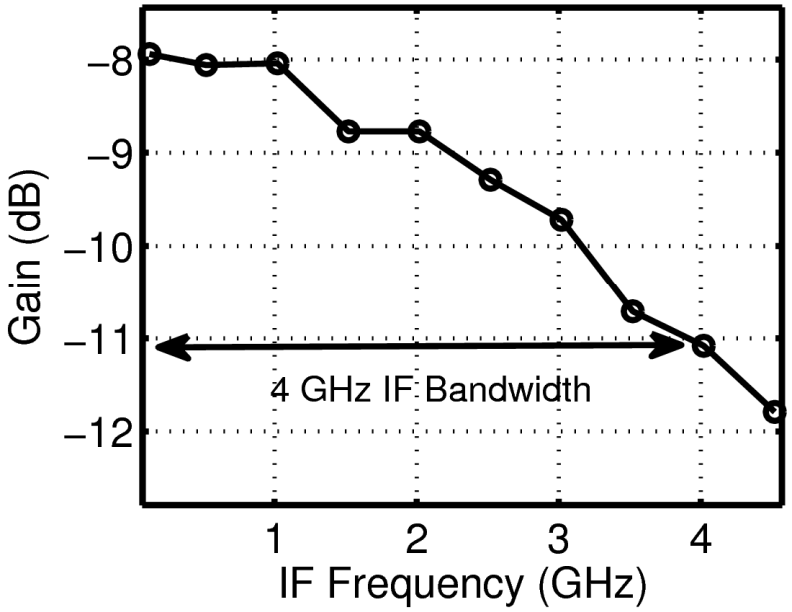


- Double Poly-Phase Filter
  - Process variations
- Symmetrical layout
  - Fine tuning with R and C
- High insertion Loss → Buffers

RF front-end (performance)

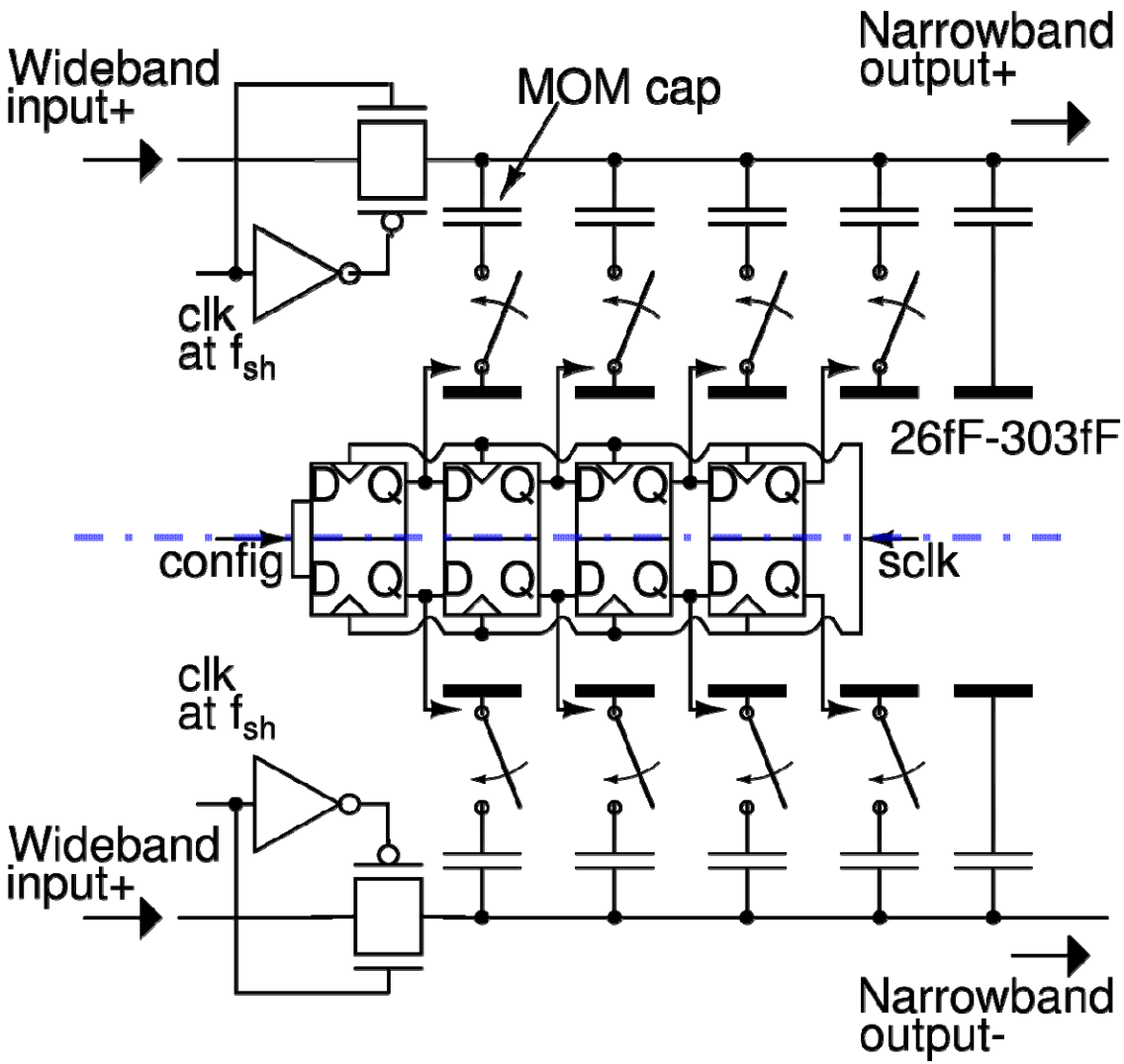
- Standalone measurements
- RF bandwidth = 7GHz, P_{FE} =88 mW
- High IF bandwidth = 4GHz





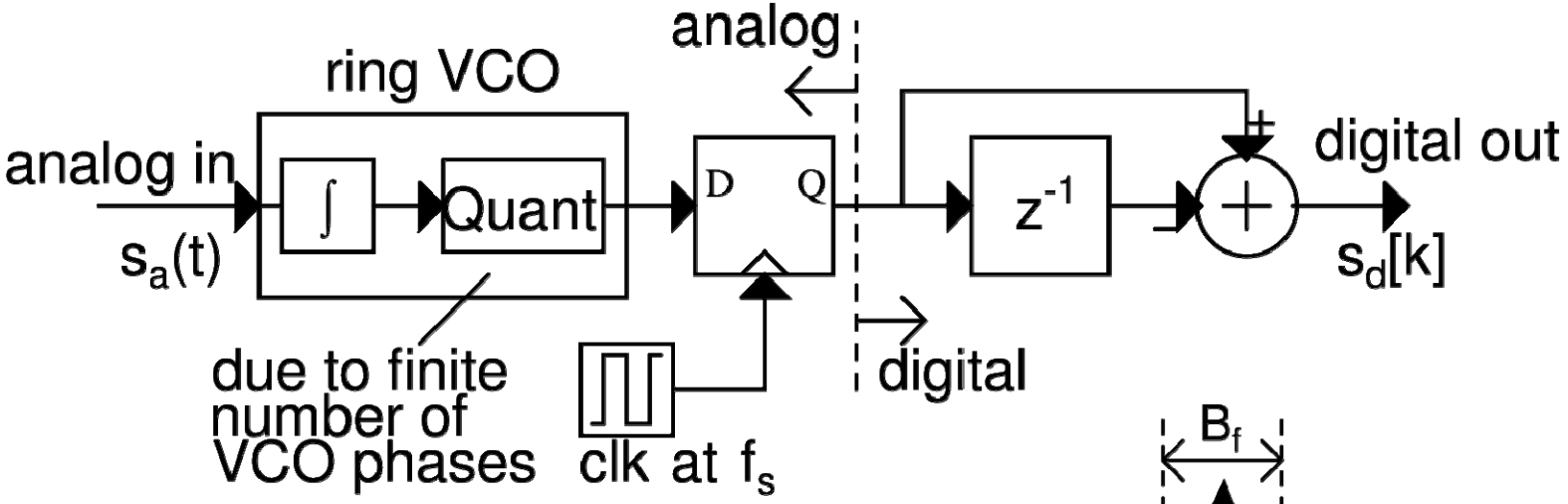
Sample-and-Hold

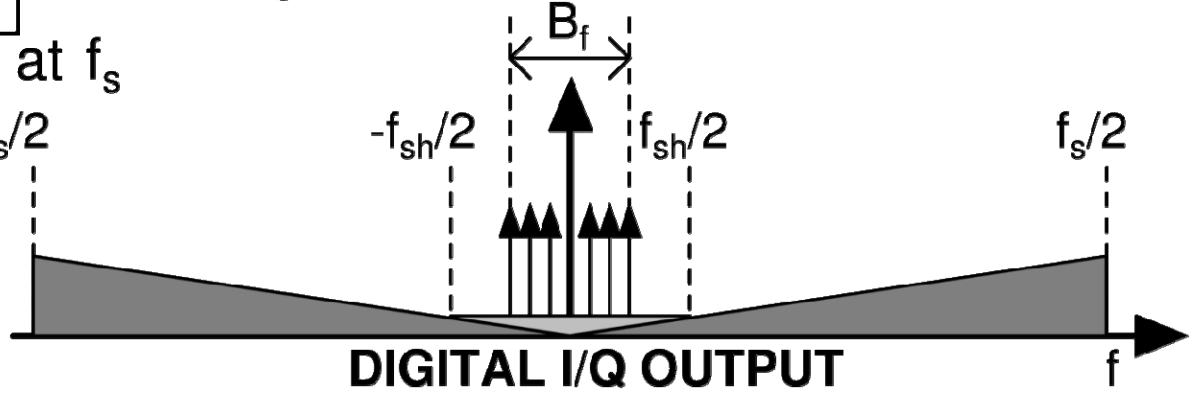
- Transmission gate S&H
- Caps
  - Trade-off:
    - Bandwidth
    - Hold-time
  - All ‘off’ here
- Symmetrical configuration



A/D (principle)

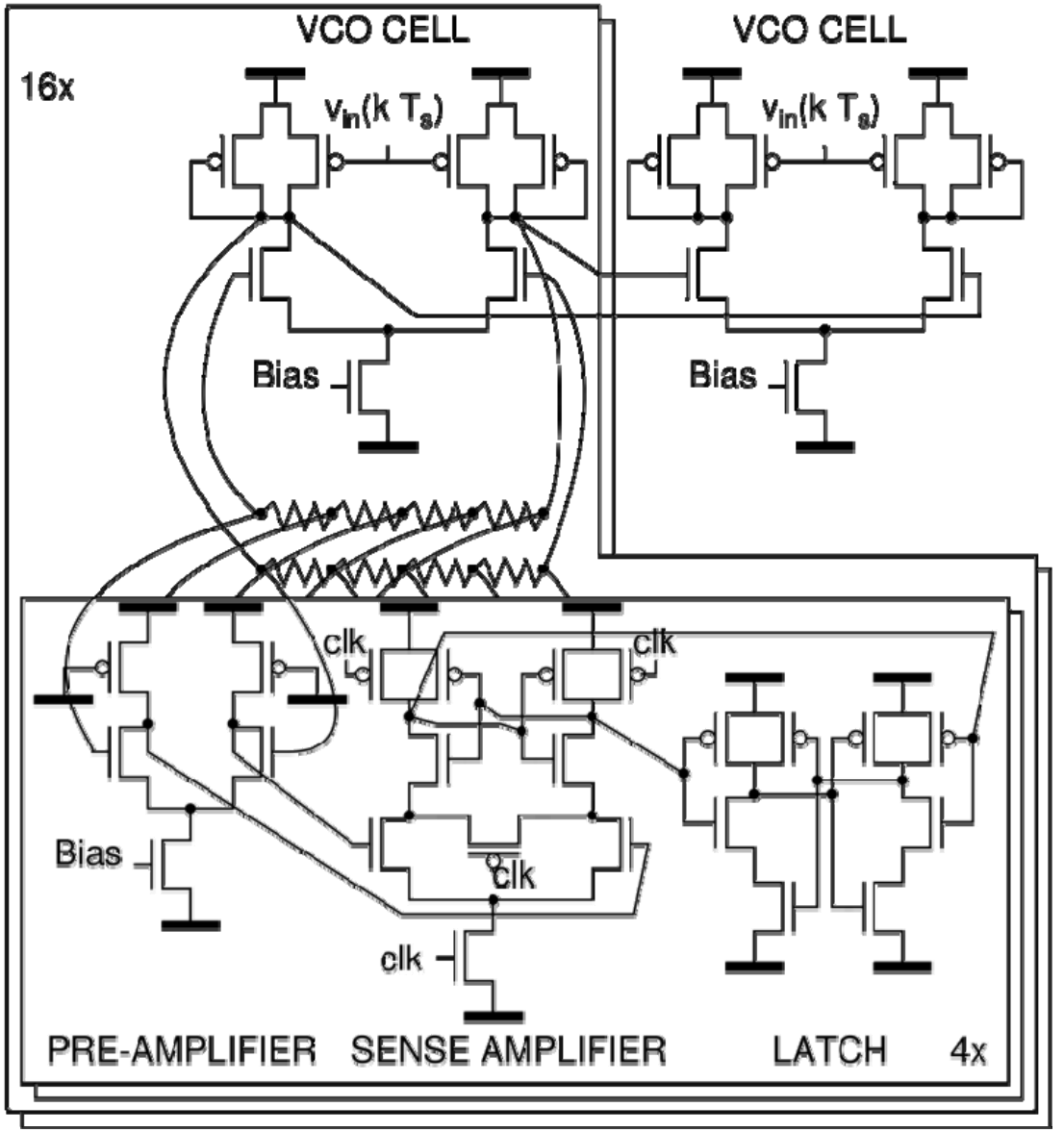
- SNR is low → use open-loop topology
- VCO-based
  - First-order noise shaping



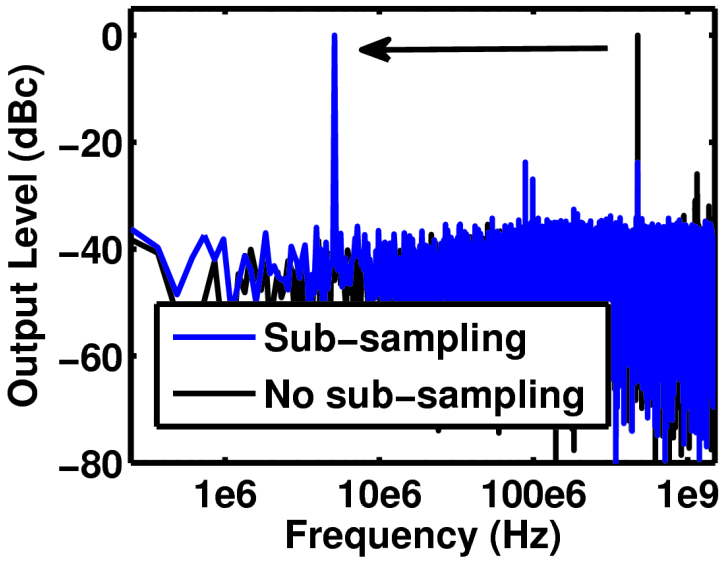


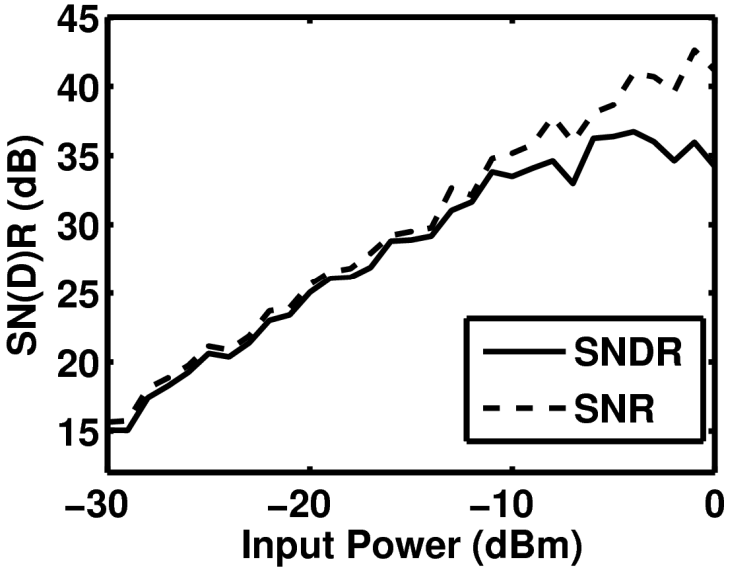
A/D (VCO)

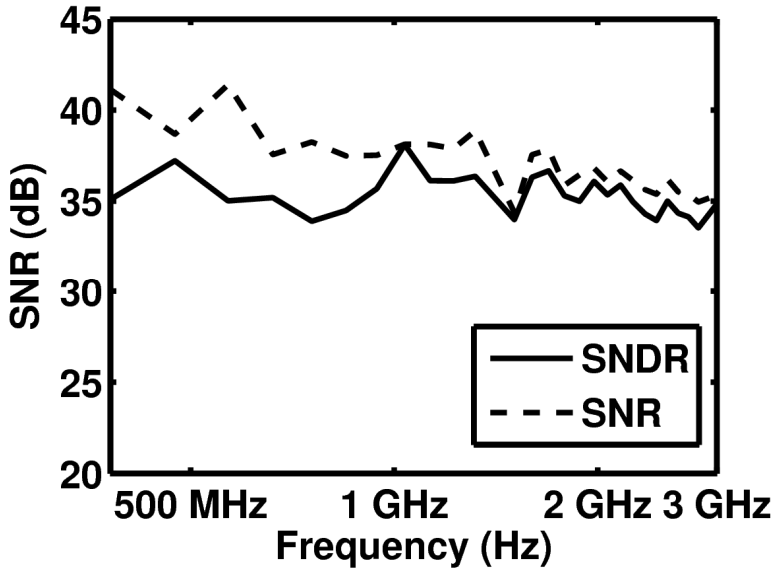
- Differential
- Interpolated
  - 16 units, 4 times interpolated = 128 phases
- Resilience to kick-back
- Sense-amplified



S&H / A/D (standalone)



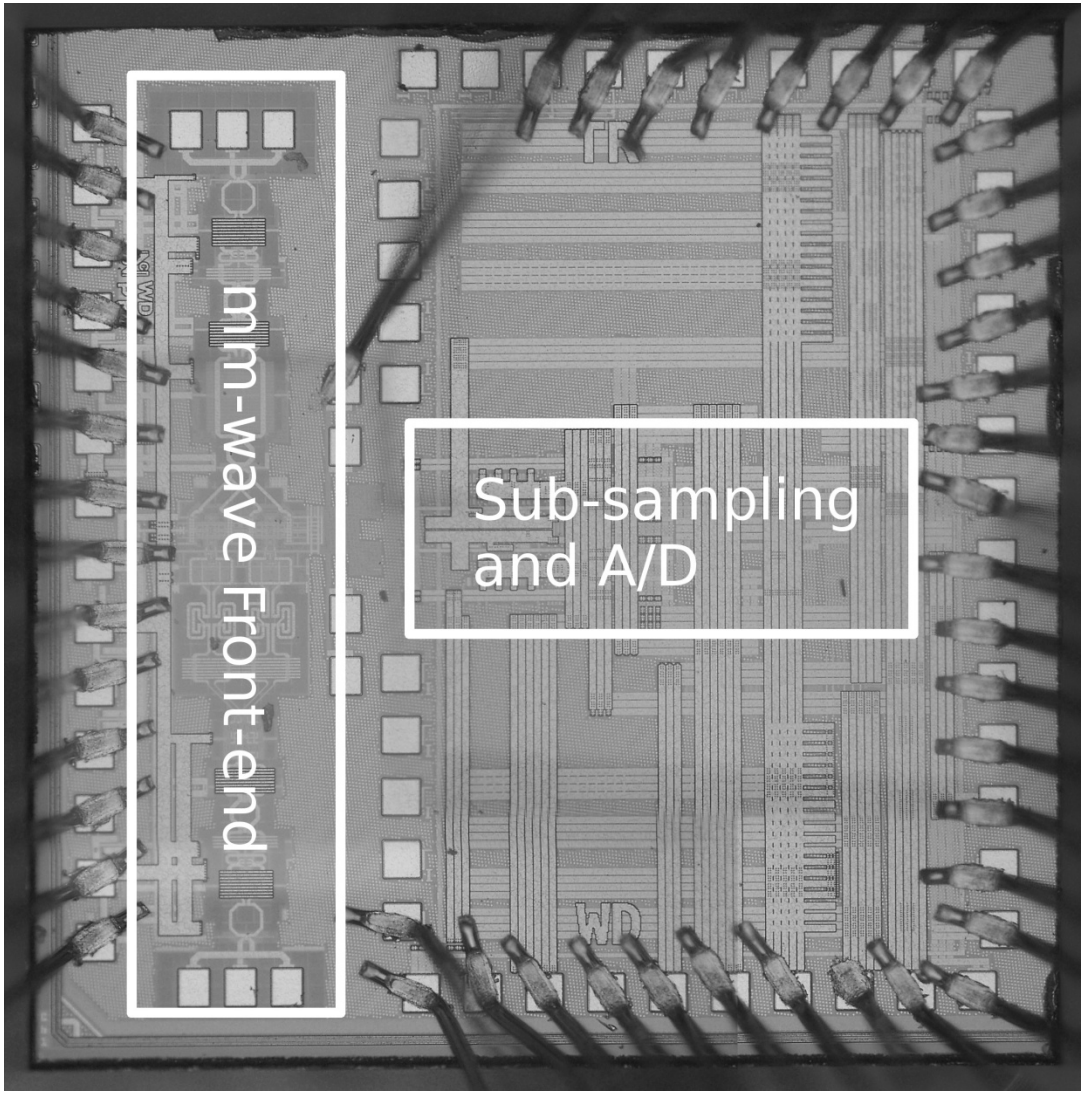




- A/D standalone measurements
- f_{sh}=187.5 MHz
- f_s=3 GHz
- $P_{A/D}$ =107 mW

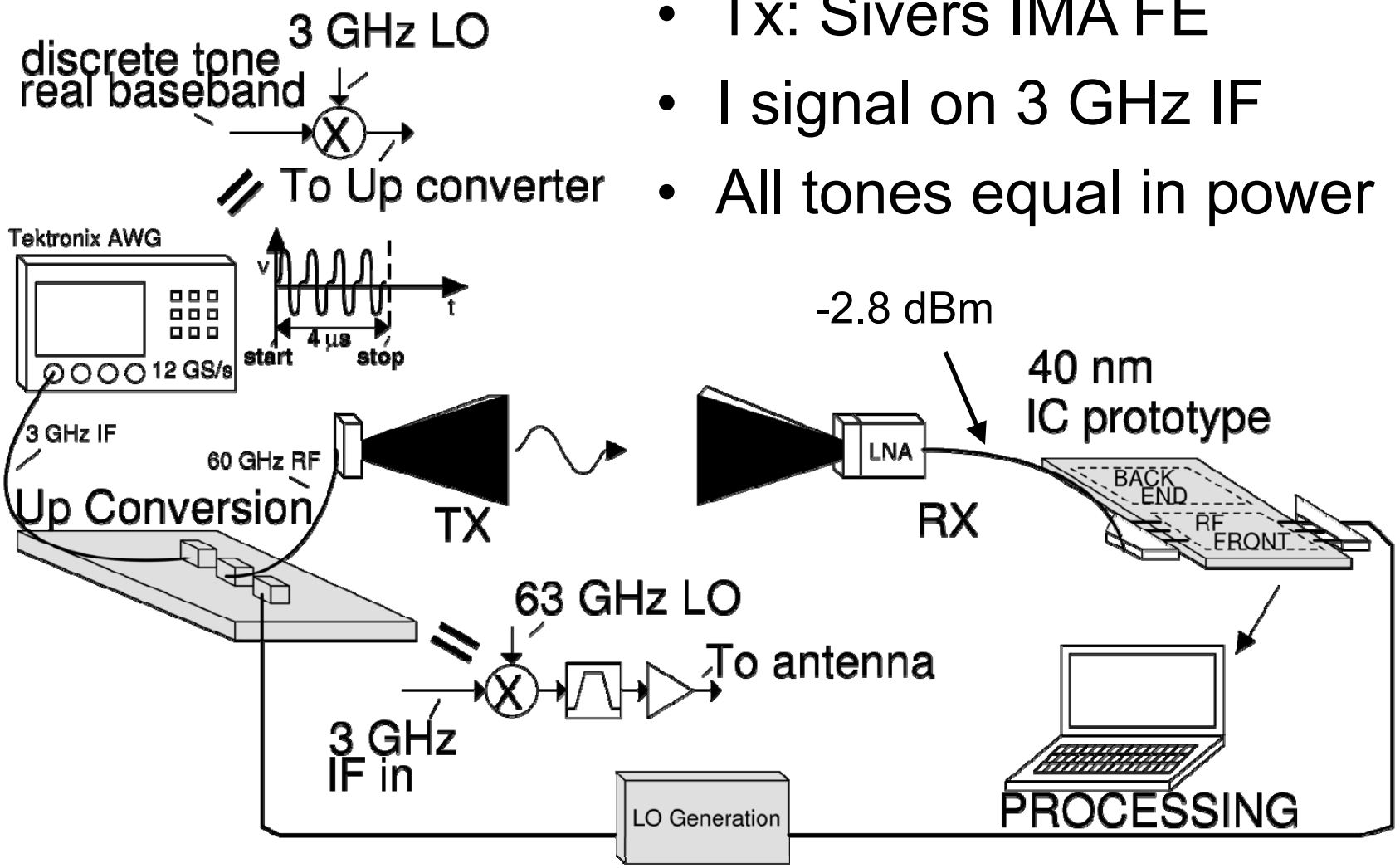
Die photograph

- 40 nm CMOS
- 2.93 mm^2
- P_{FE} =88 mW
- $P_{A/D}$ =107 mW

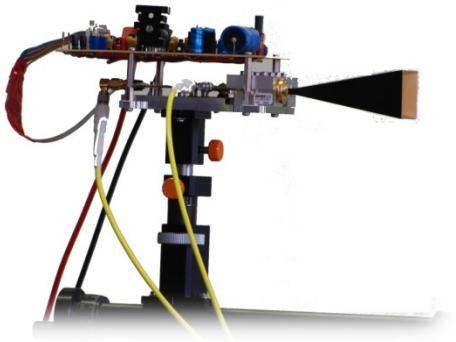


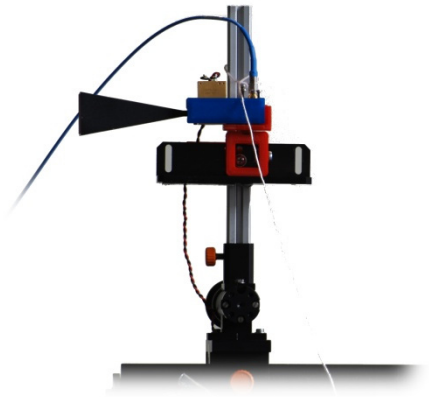
Measurement setup

- Tx: Sivers IMA FE
- I signal on 3 GHz IF
- All tones equal in power



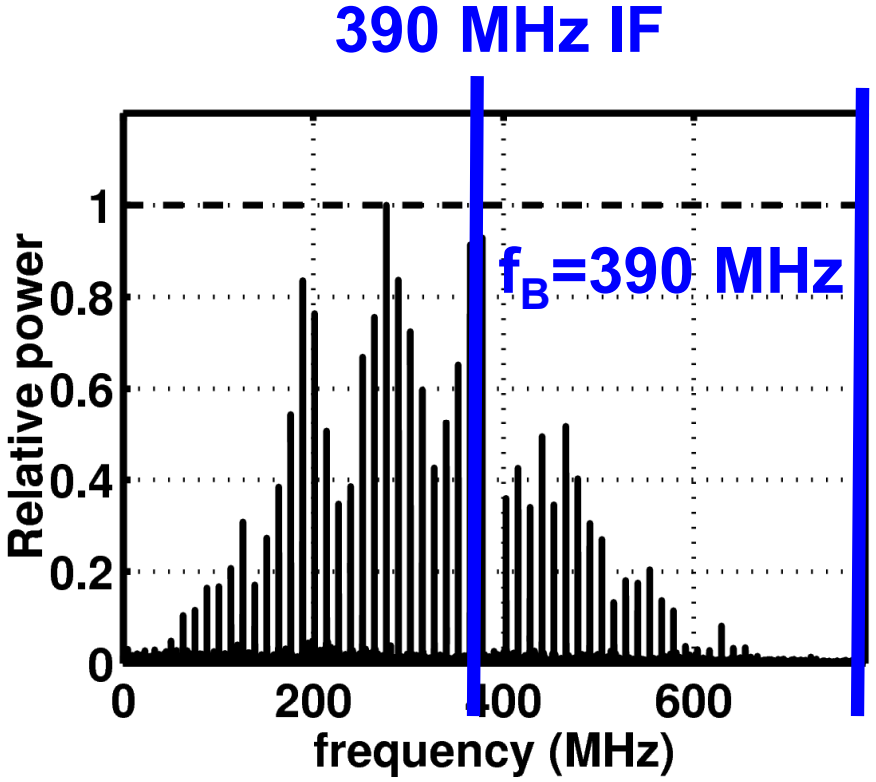
Measurement setup

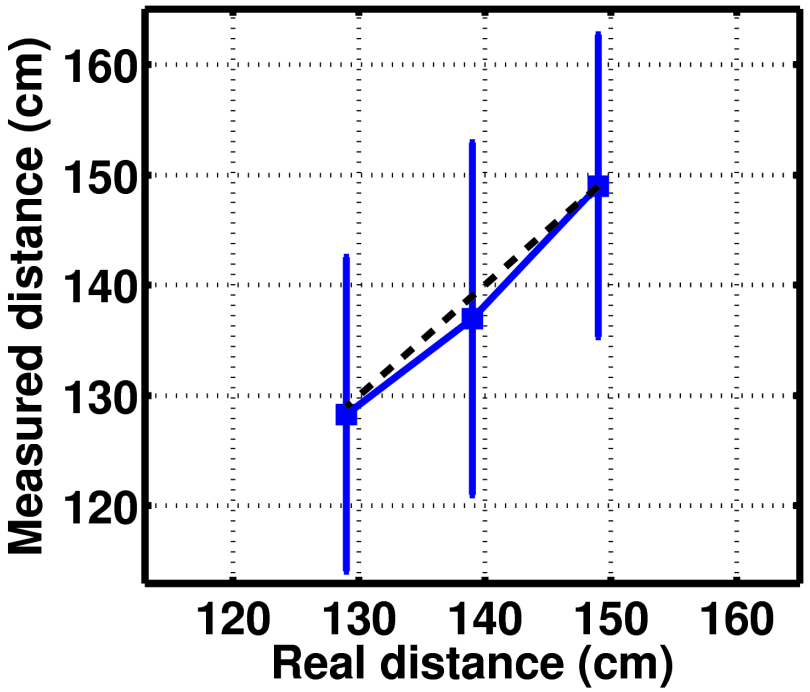




Modulated carrier measurements

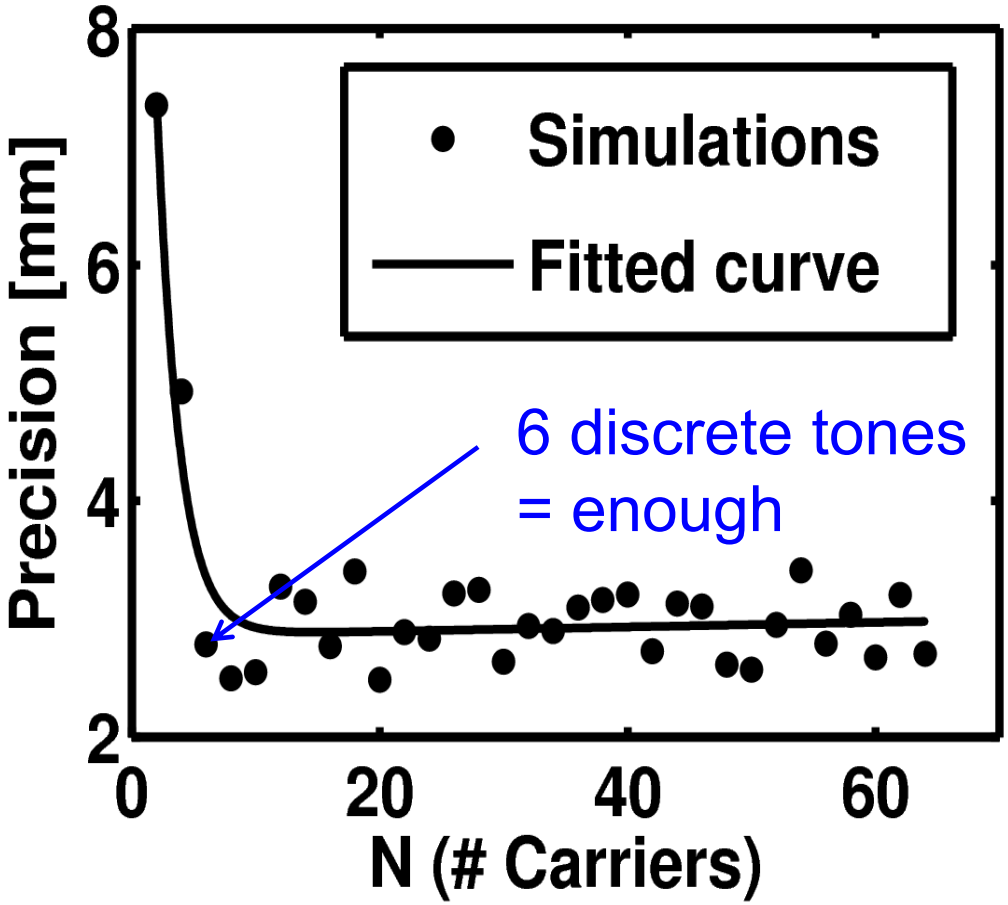
- PRBS-5 sequence (xcorr.)
- T=12 μs, $f_{sh}=f_s=2$ GHz
- No sub-Nyquist sampling





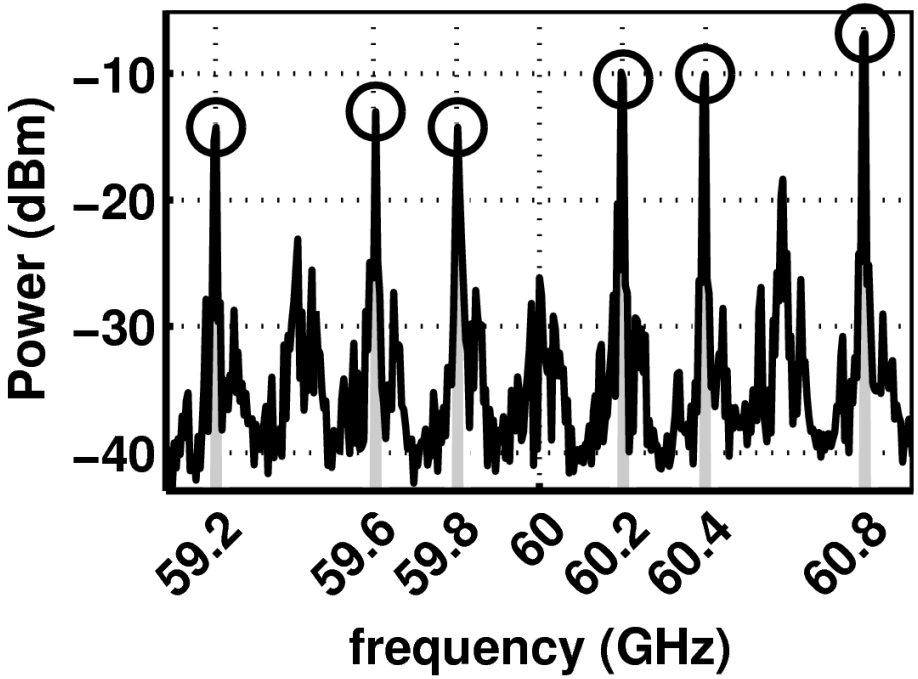
Determining the number of tones

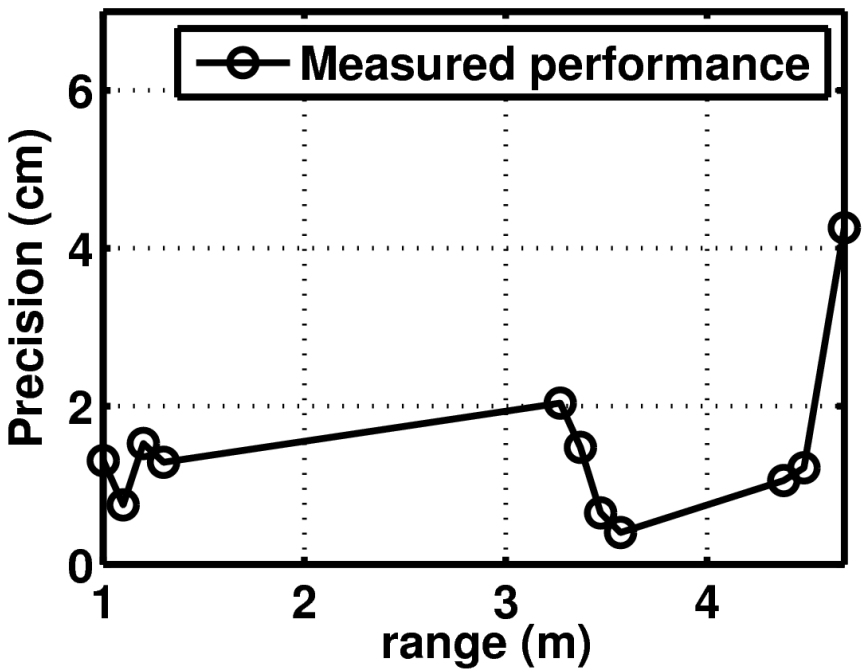
- BW = 1.6 GHz, T = 4 µs



Measurements

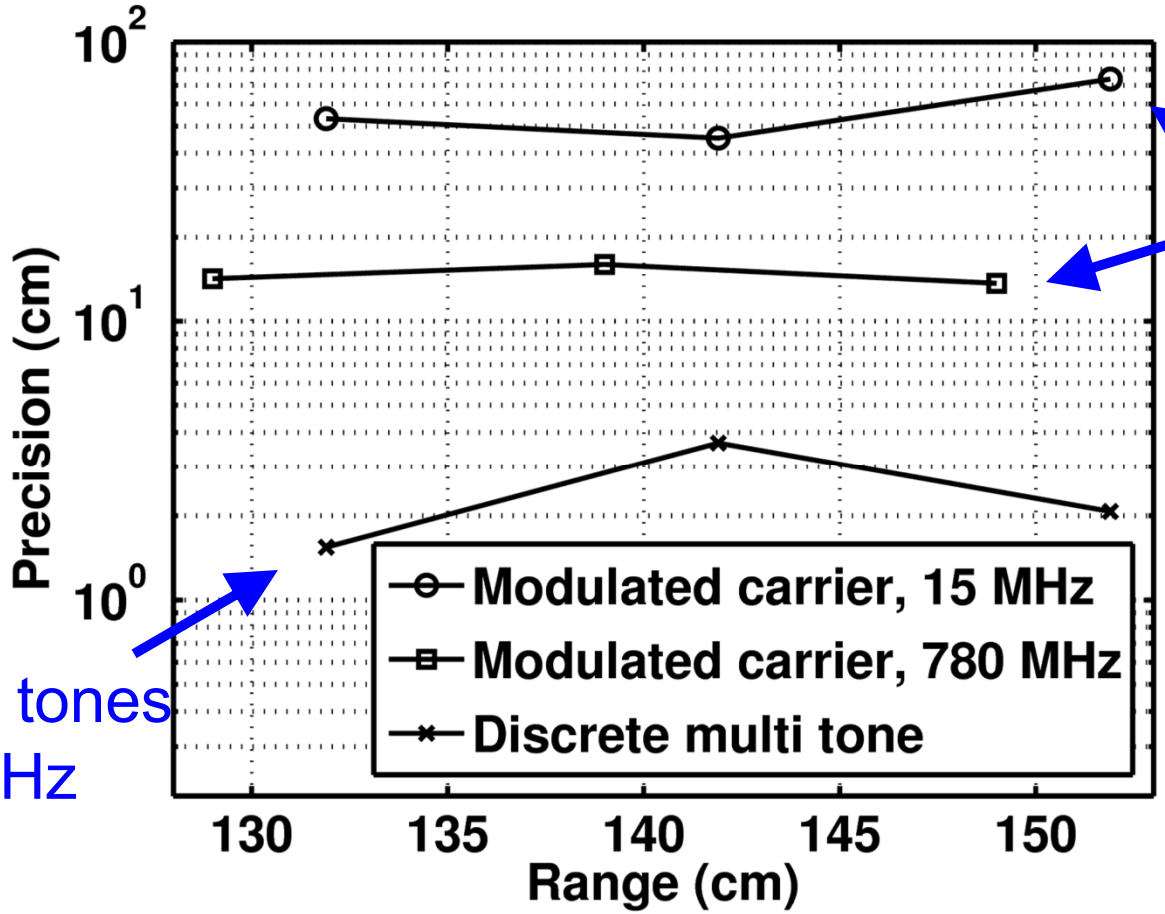
- 6 tones, BW=1.6 GHz, T=5x4 µs
- f_{sh}=187.5 MHz → BW_f=60 MHz (f_s=3 GHz)



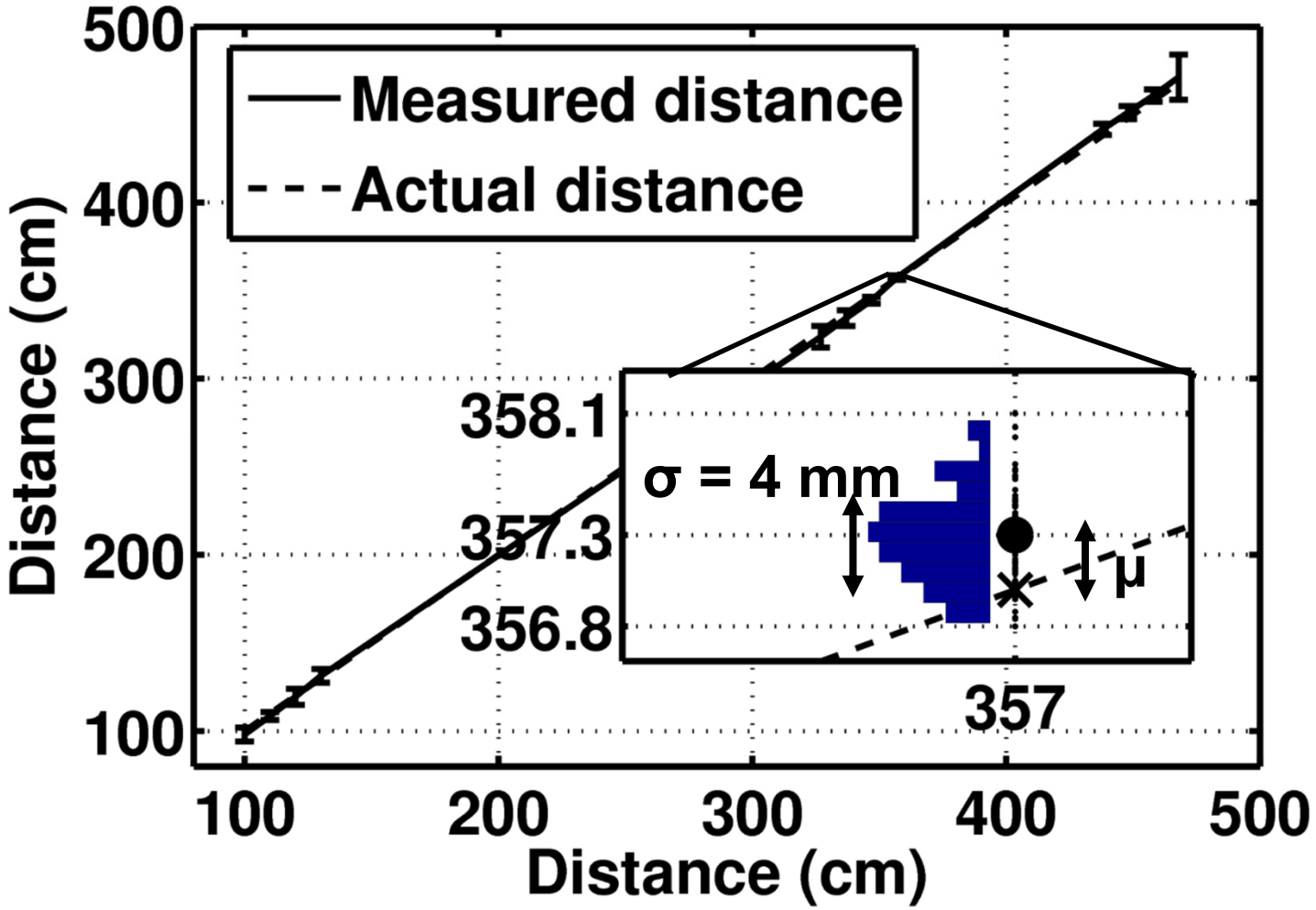


Measurements

- Compared to modulated carrier (PRBS-5)
- No sub-sampling: T=12 μs, f_s=2 GHz

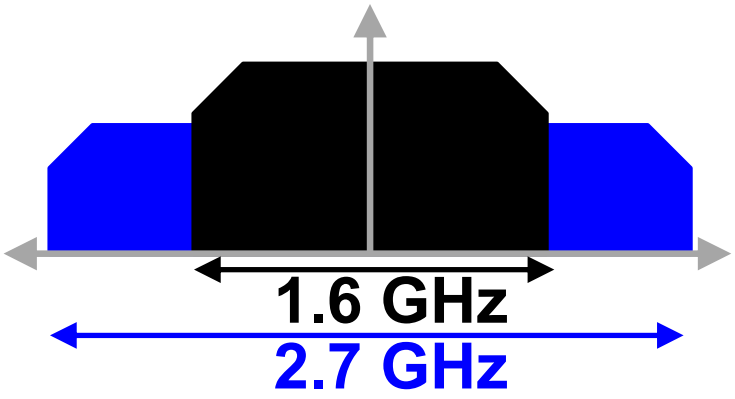


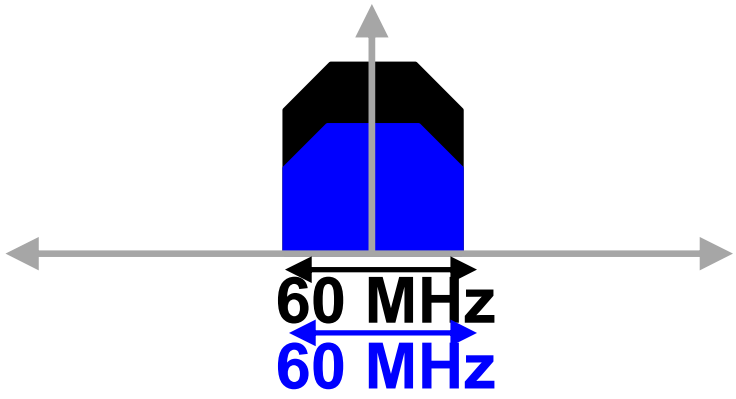
Measurements

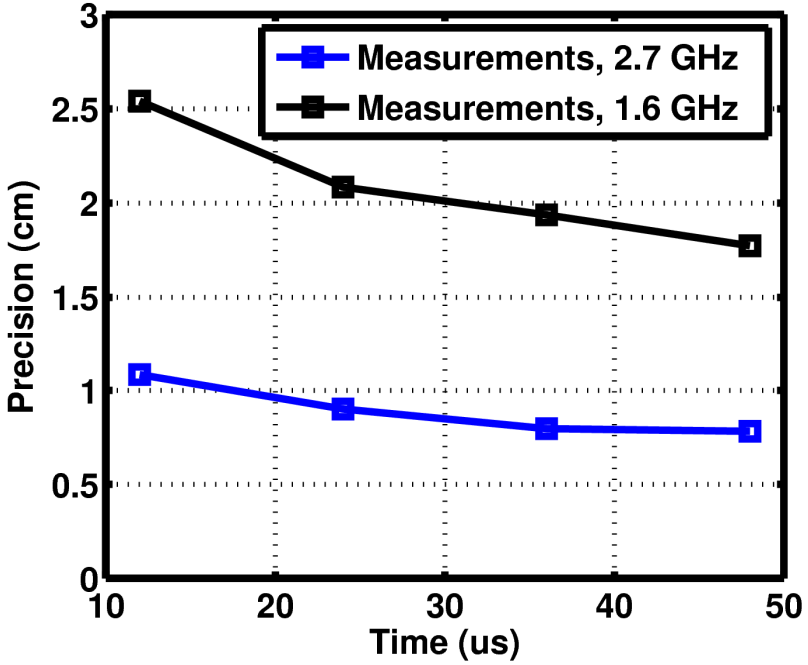


T=20 μs, f_{sh}=187.5 MHz, f_s=2 GHz

Extension of bandwidth







- 6 tones
- Range=1.37 m
- f_{sh}= 125 MHz
- f_s= 2 GHz

	This Work	[JSSC2010]	[ISSCC2012]	[ISSCC2013]
Features	**Multi-tone, bandwidth-reducing**	FMCW	SAR frequency sweep	Equivalent time-sampling
Max measured range	**5m**	≈100m	1.2m	N/A
Precision	**4mm @ 3.6m (measured)**	< 100mm @ 10 m (measured)	7.6mm @ >1m (measured)	Depth resolution 1.5mm (theoretical)
Power Consumption	**195mW**	> 100mW	214mW	76mW
Frequency Band	**60GHz (V-band)**	77GHz (W-band)	144GHz (D-band)	10GHz
Bandwidth	**2GHz**	700MHz	400MHz	7.3GHz
Package Duration	**20µs**	1.5ms	2µs	1.5µs
Signal Type	**Multi-Tone**	FMCW-sweep	Single Tone	Wideband
Tx-Rx LO phase relation theoretically needed?	**NO**	NO	YES	YES
External LO	**YES**	NO	NO	NO
CMOS Tech.	**40nm**	65nm	65nm	65nm

Conclusions

- 60 GHz receiver in 40 nm CMOS
  - Front-end + sub-sampling + I/Q A/D
- Exploiting discrete-carrier ranging
- Bandwidth reduction thanks to sub-sampling
- Coexists with custom algorithm
- Precision of 4 mm
- Enabling update rates of 50 kHz

A 16TX/16RX 60GHz 802.11ad Chipset with Single Coaxial Interface and Polarization Diversity

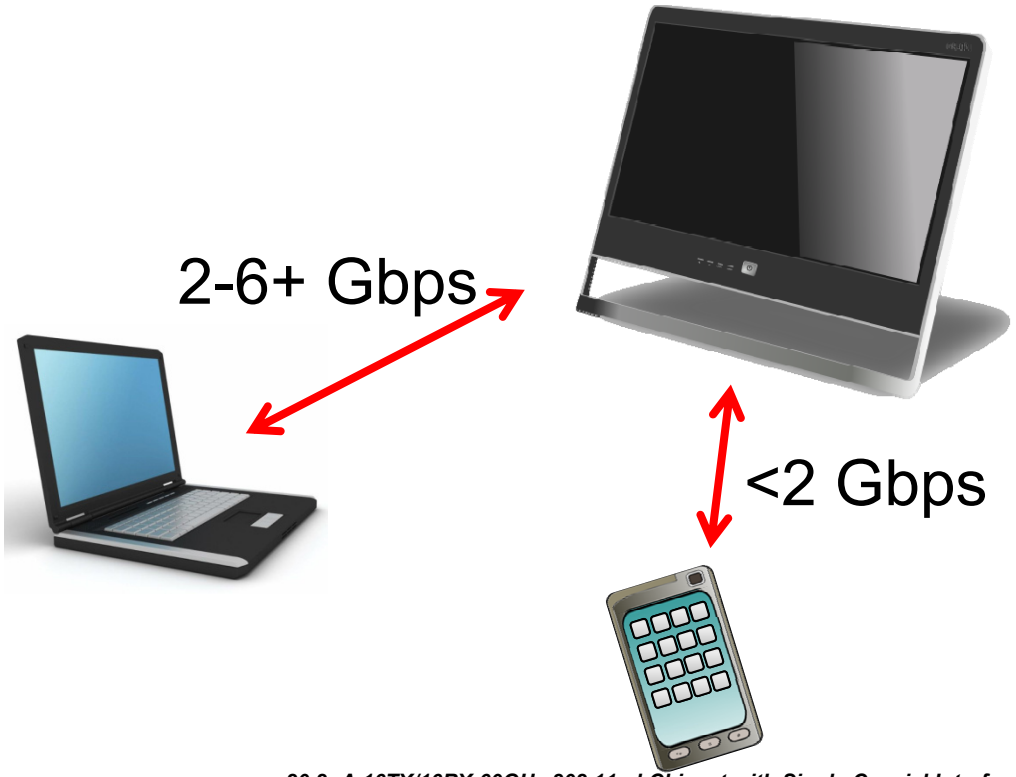
M Boers, I Vassiliou, S Sarkar, S Nicolson, E Adabi, B Afshar, B Perumana, T Chalvatzis, S Kavadias, P Sen, W L Chan, A Yu, A Parsa, M Nariman, S Yoon, A Grau Besoli, C Kyriazidou, G Zochios, N Kocaman, A Garg, H Eberhart, P Yang, H Xie, H J Kim, A Tarighat, D Garrett, A Blanksby, M K Wong, D P Thirupathi, S Mak, R Srinivasan, A Ibrahim, E Sengul, V Roussel, P-C Huang, T Yeh, M Mese, J Castaneda, B Ibrahim, T Sowlati, M Rofougaran, A Rofougaran

Why 60GHz?

- **High throughput !**
- ~8GHz BW available on 2GHz channels
- Standardized – 802.11ad

Why 60GHz?

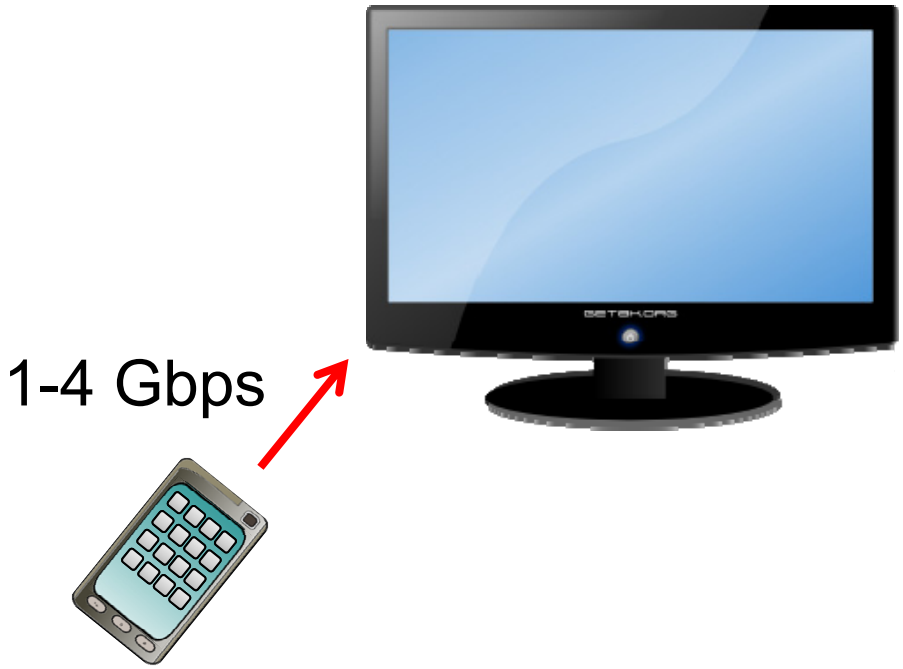
- **High throughput !**
- ~8GHz BW available on 2GHz channels
- Standardized – 802.11ad



Monitor / Dock
Gigabit Ethernet
USB3

Why 60GHz?

- **High throughput !**
- ~8GHz BW available on 2GHz channels
- Standardized – 802.11ad

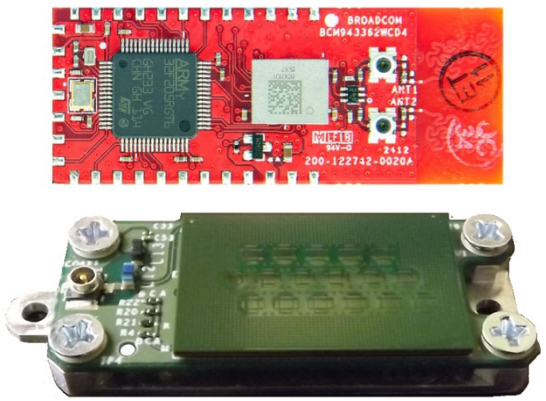


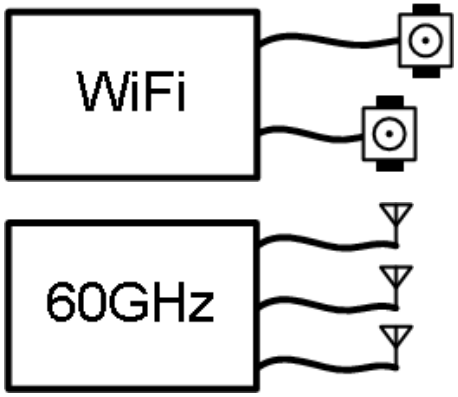
Outline

- Challenges
- Link budget
- System overview
- PA, LNA and TRX+P
- Radio calibration
- Antenna and package
- Results

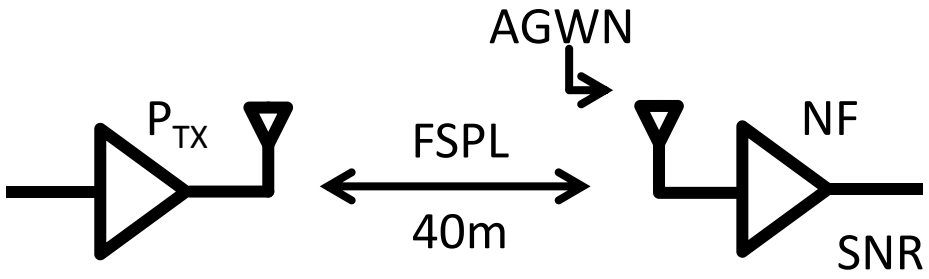
Challenges

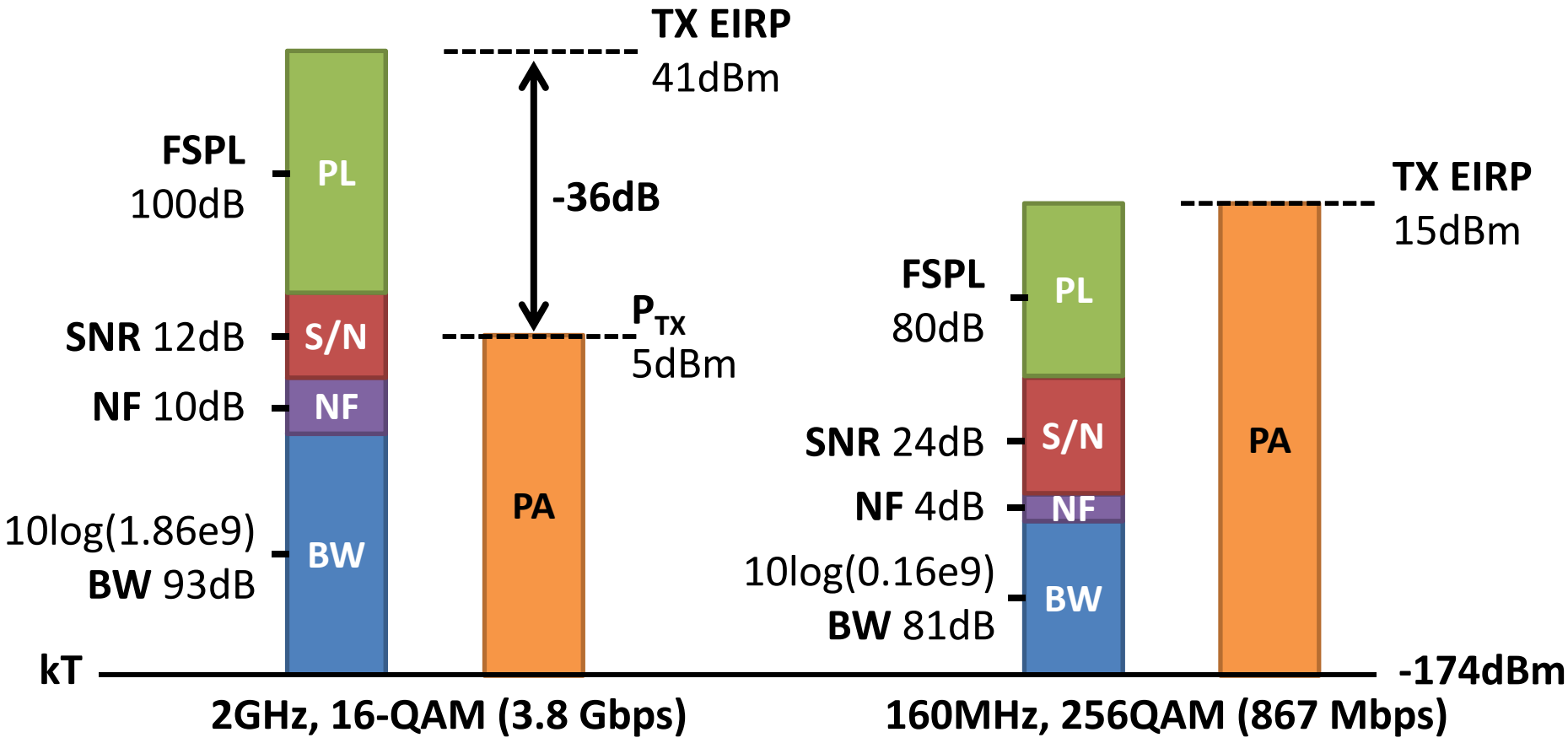
- CMOS implementation
  - Variation, f_t/f_{max}, lossy substrate
- Propagation loss
- Antenna and placement in platform
- High volume test





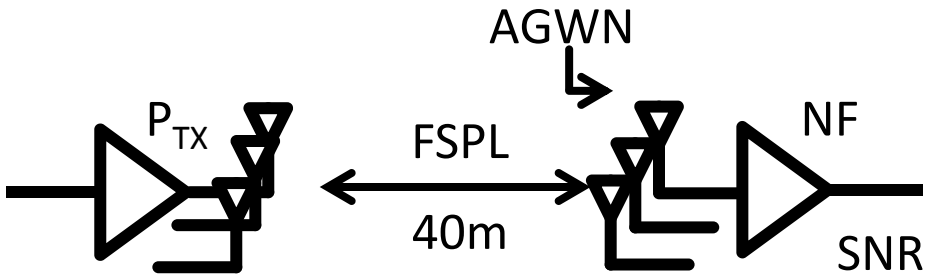
60GHz link

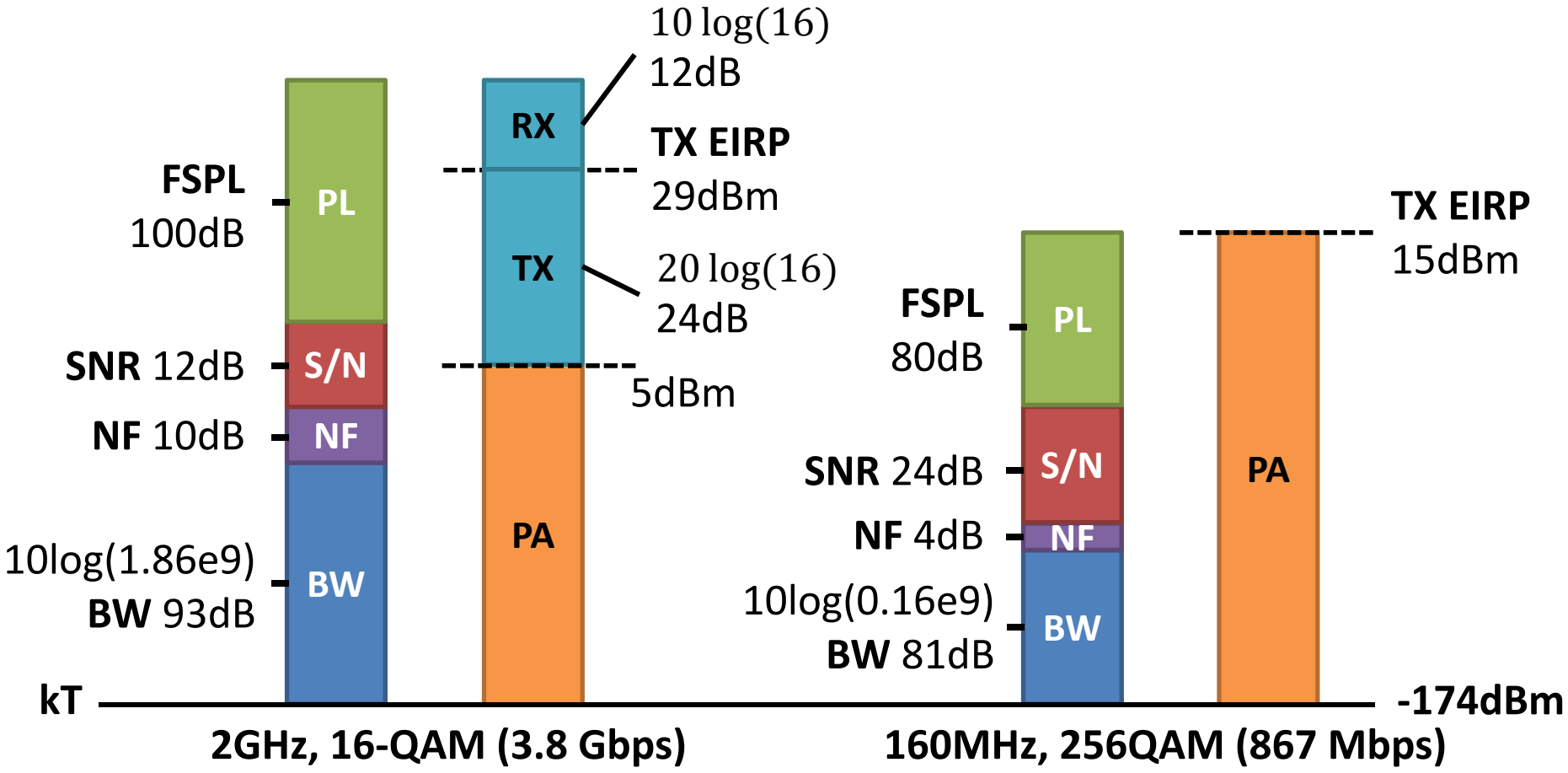




Adapted Natarajan *JSSC May 11*

60GHz link





Adapted Natarajan *JSSC May 11*

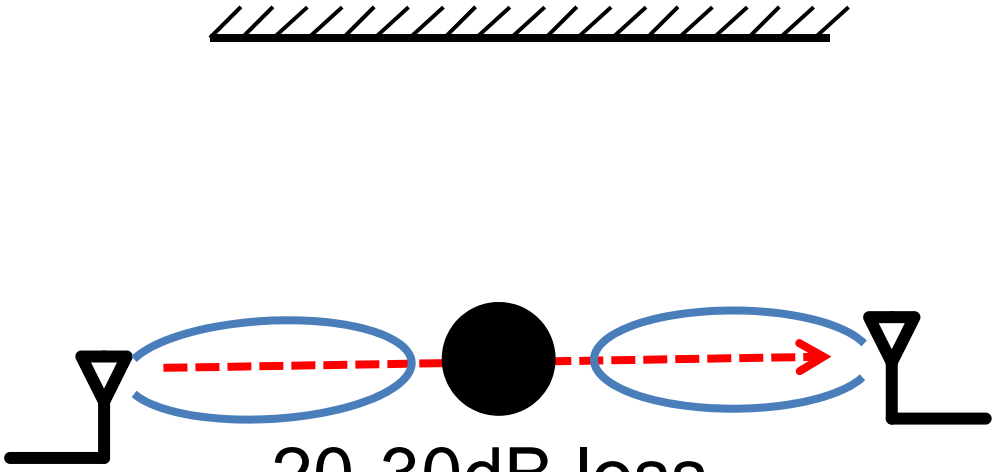
60GHz link - beamforming

40m LOS
3.8 Gbps (MCS11)

- Rarely have LOS for 60GHz link
- Need to look at NLOS performance

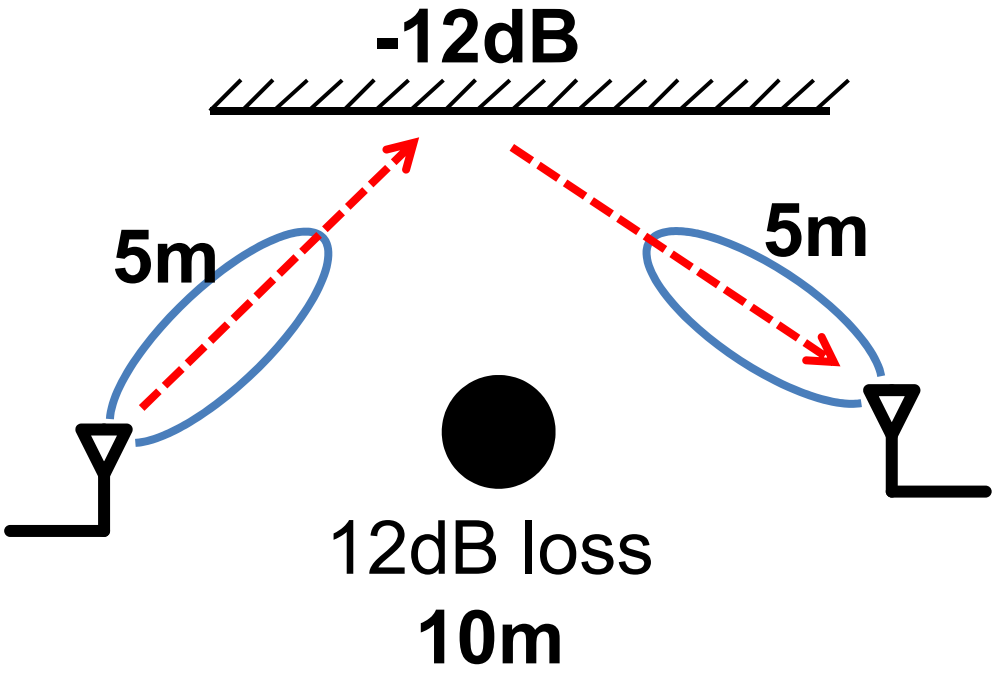
Natarajan *JSSC May 11*
Gustafson *Ant & Prop Mar 12*
Maltsev *JSAC Aug 09*

60GHz link - beamforming



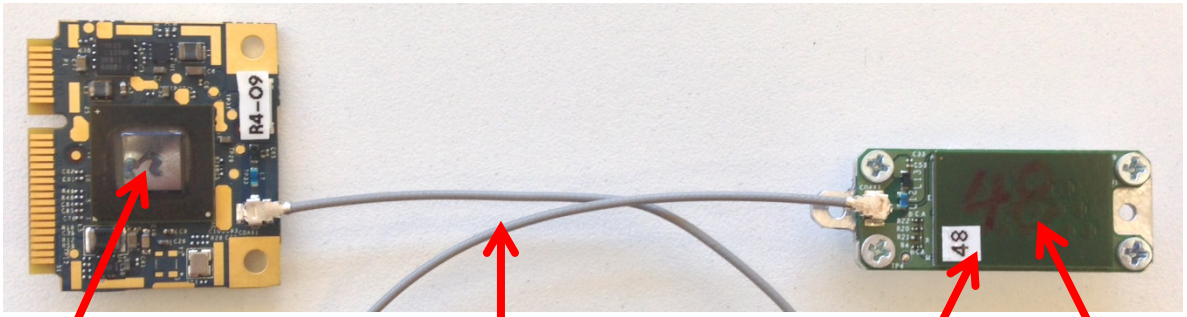
- Human body loss 20-30dB+

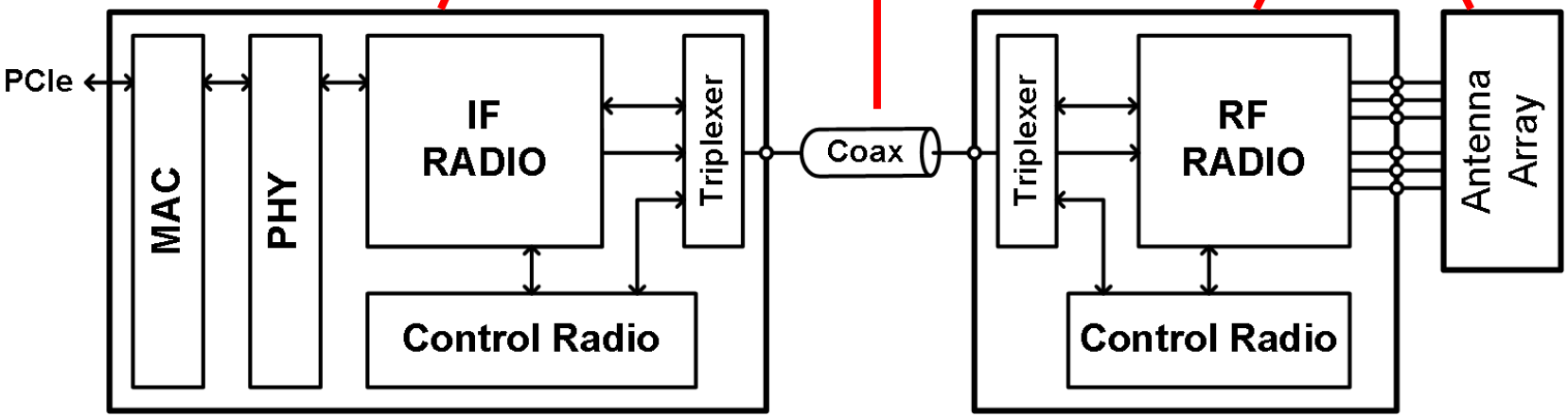
60GHz link - beamforming



- Use beamforming to steer around blockers
- Reflection loss typically less than blocker loss

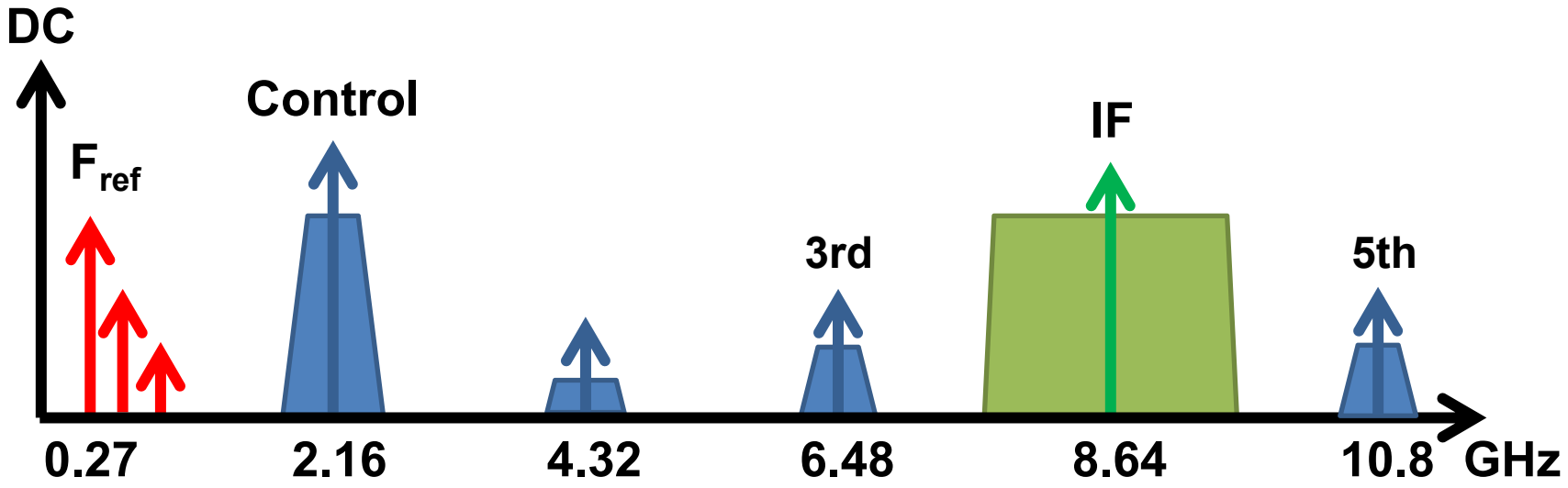
System Overview

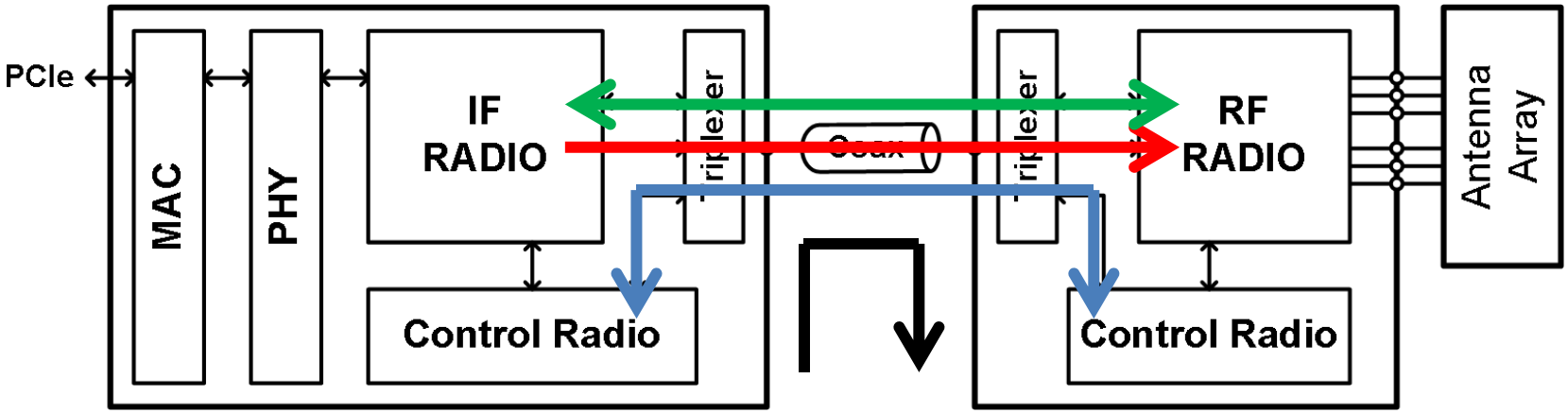




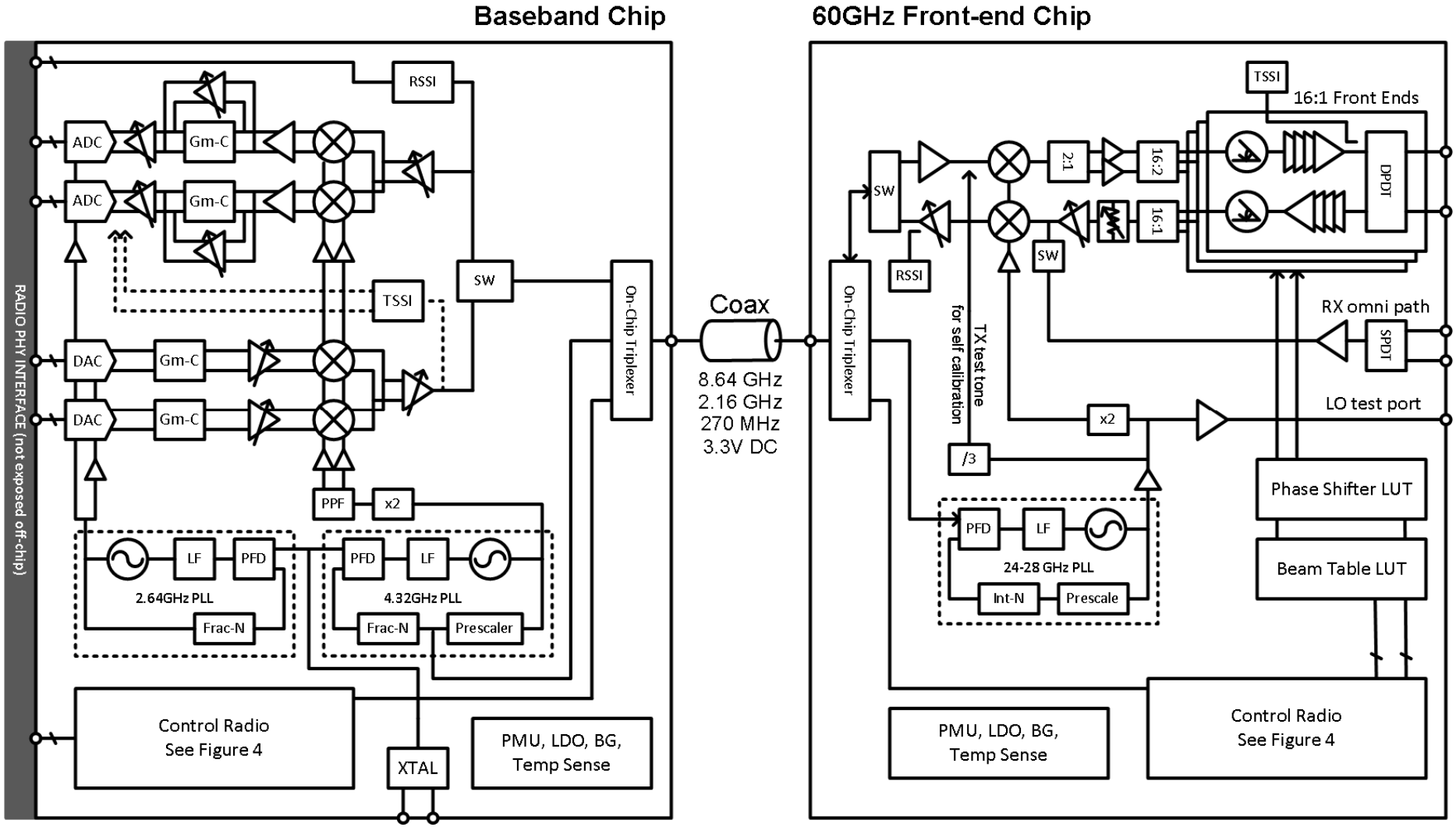
- Dual chip architecture, single coax
- 16x16 elements, TRX+P
- Calibration, self-test, PVT tolerant design

Frequency Planning

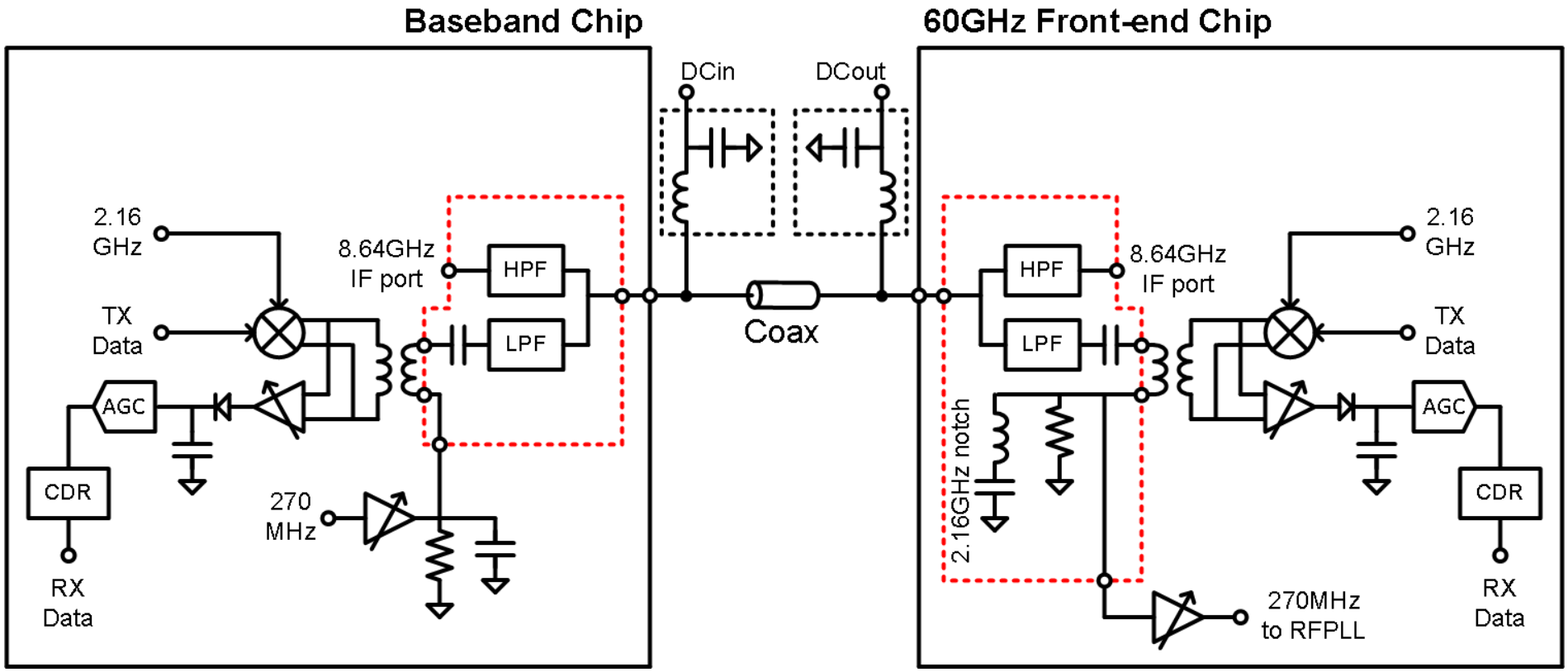




Radio Block Diagram

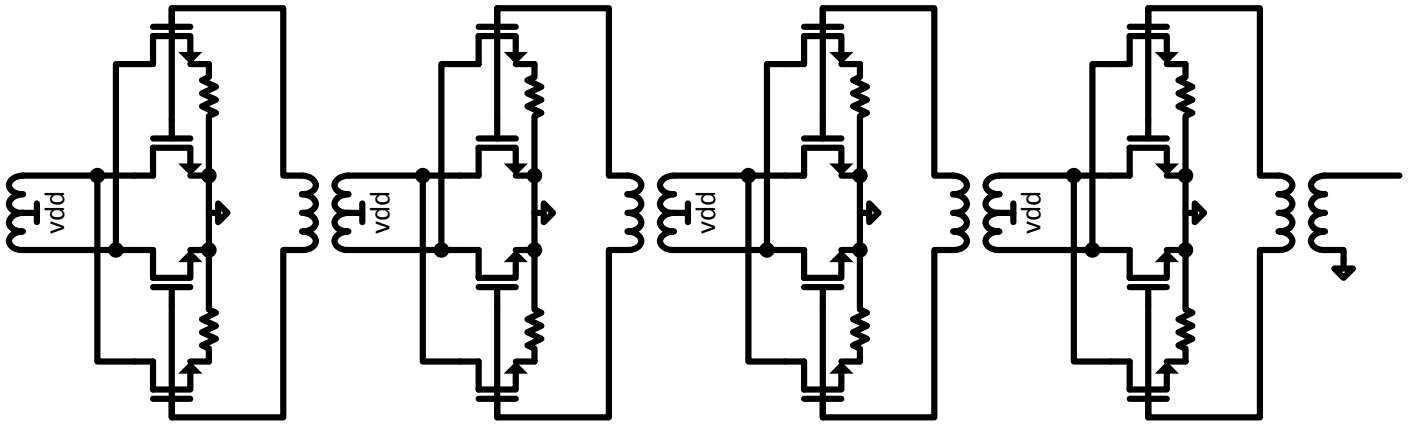


Control Radio Block Diagram

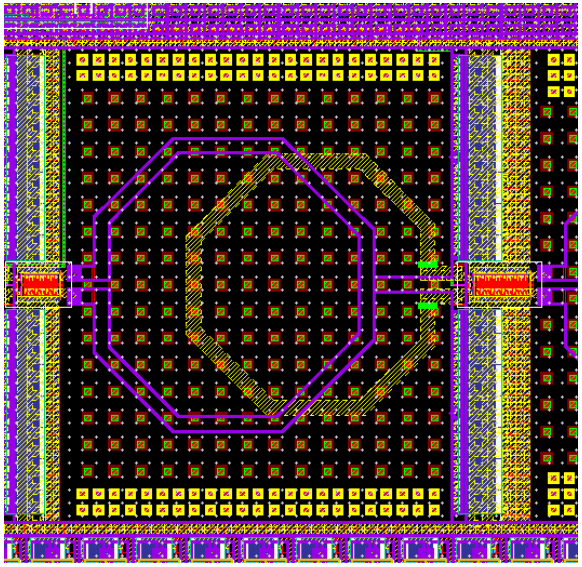


- Enables simple placement
- Control radio: target $10e^{-12}$ BER

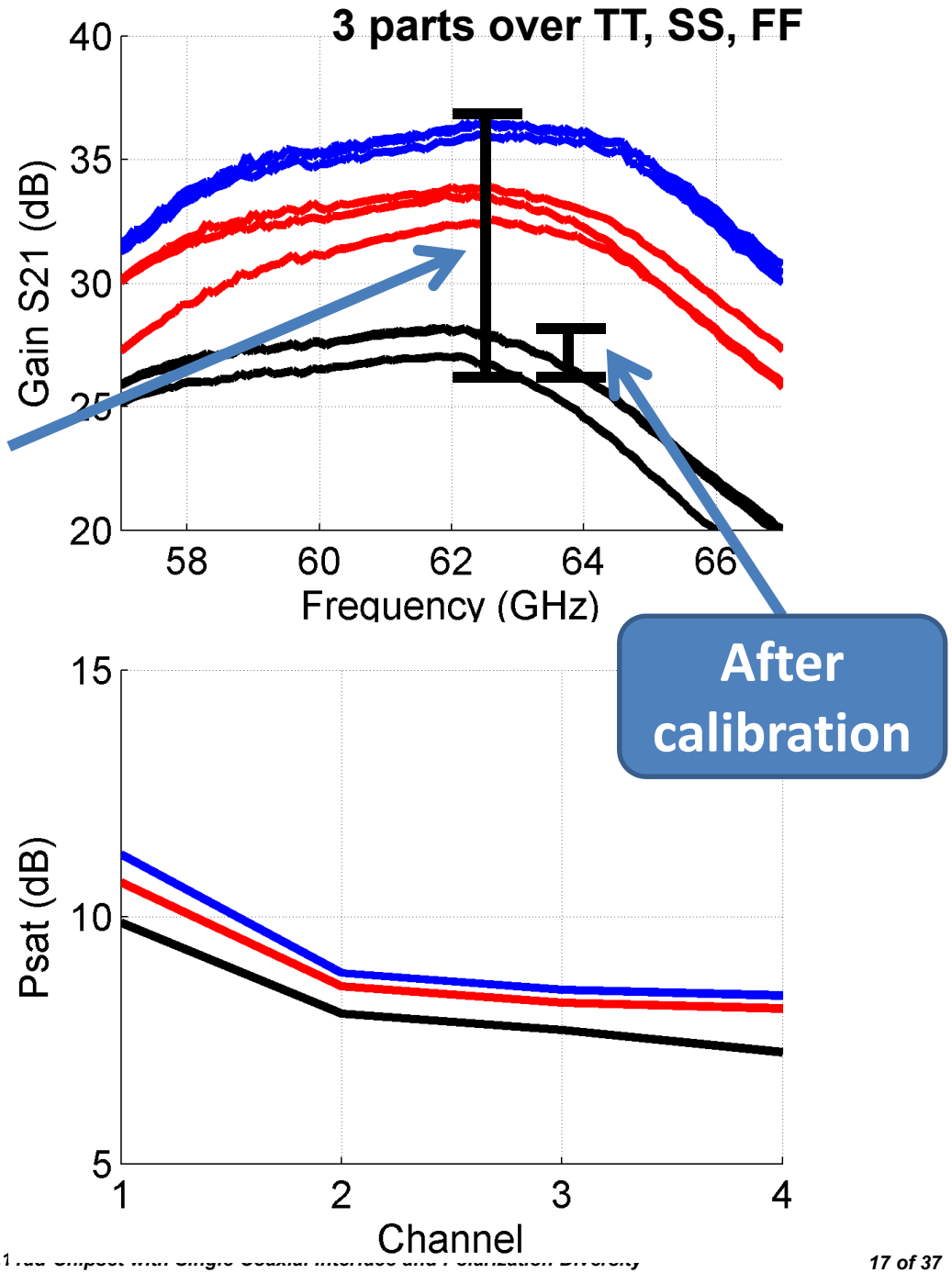
Power Amplifier



- Differential 4-stage
- Low-k transformers
- Staggered tuning
- Wide BW
- MOS neutralization

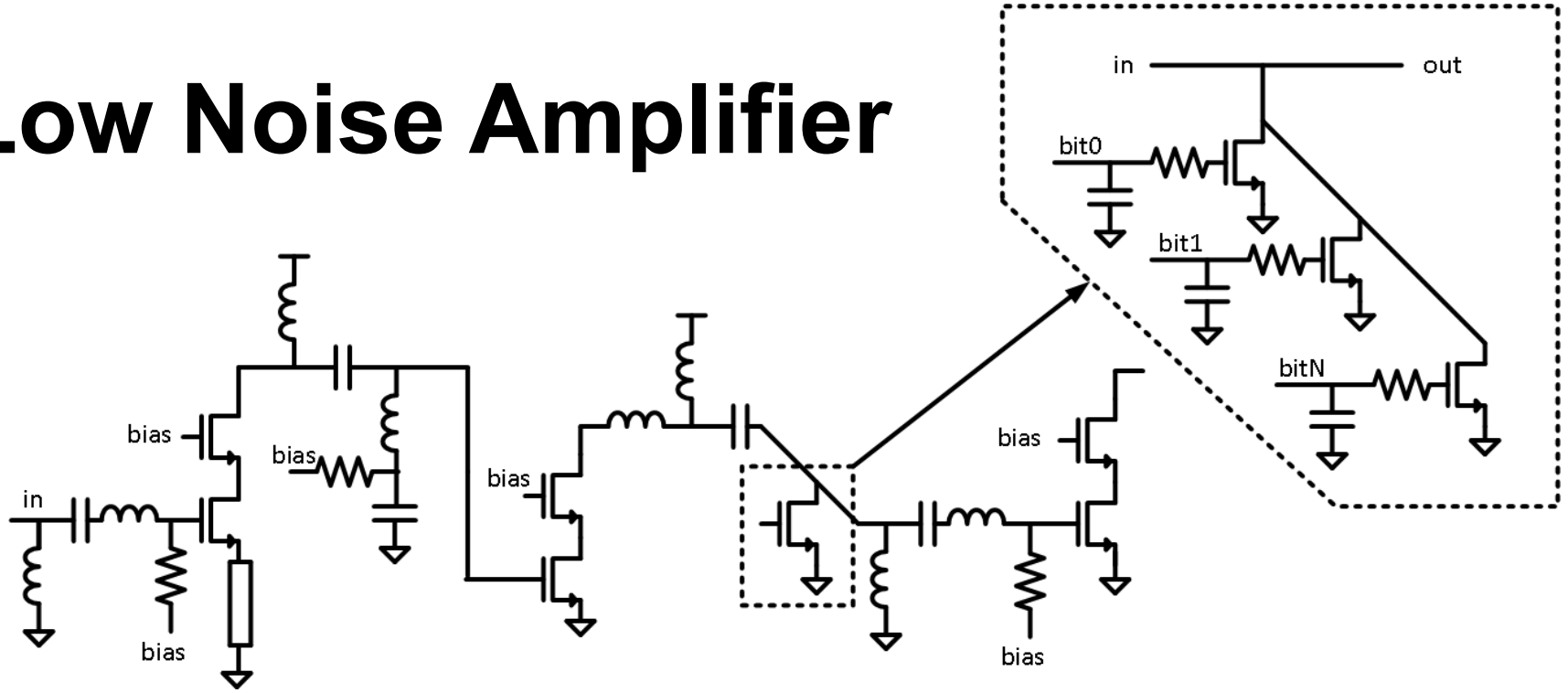


PA Results

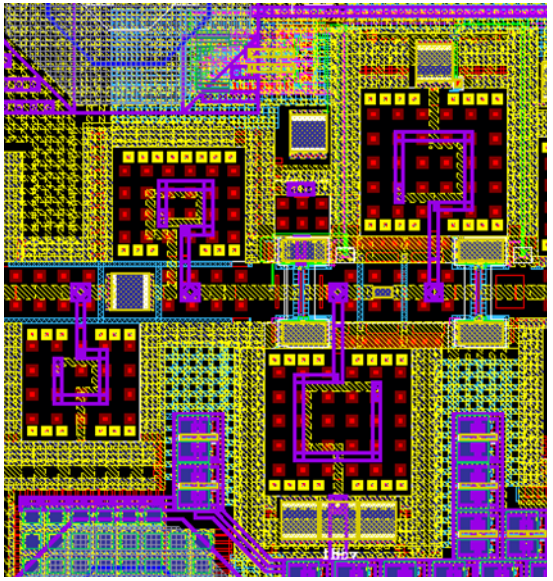


Parameter	Value
p1dB	5.5 dBm
P_{sat}	8 dBm
Gain	>25 dB
S22	< -10 dB
Power	45mW
PAE @ p1dB	7.8%
Area	0.25mm^2

Low Noise Amplifier

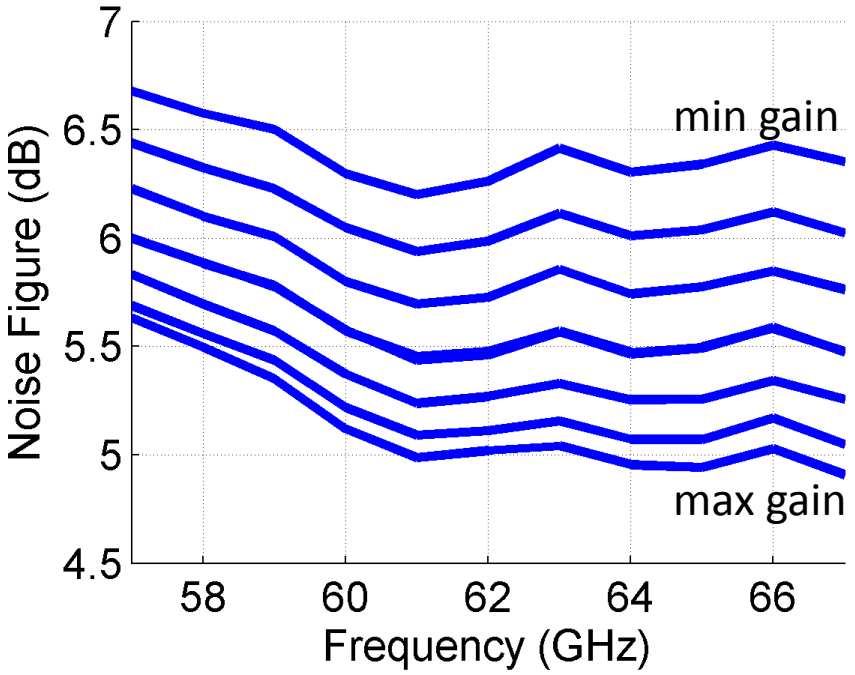


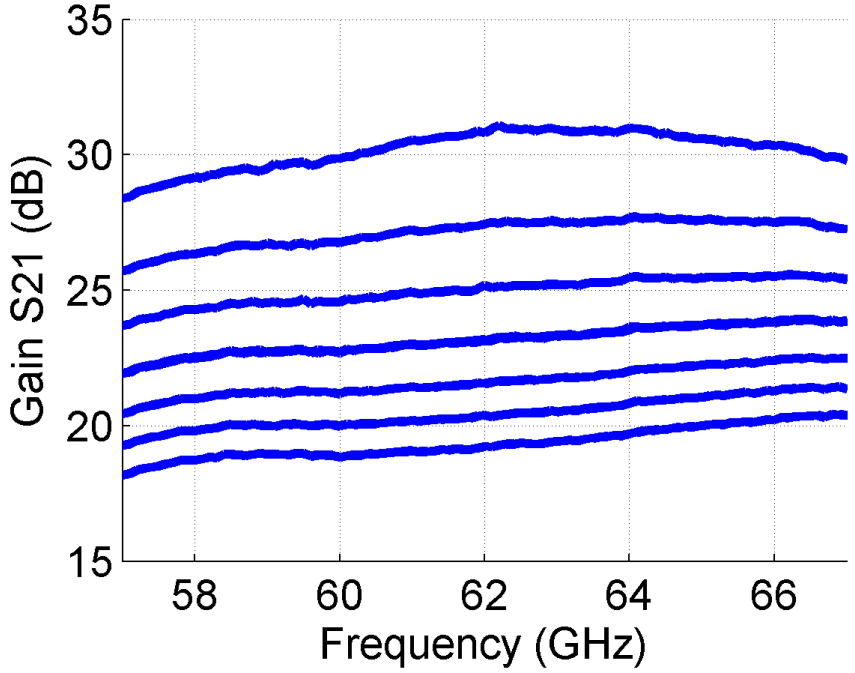
- Single-ended 4-stage
- L-C-L matching
- VGA using switched NMOS in triode region



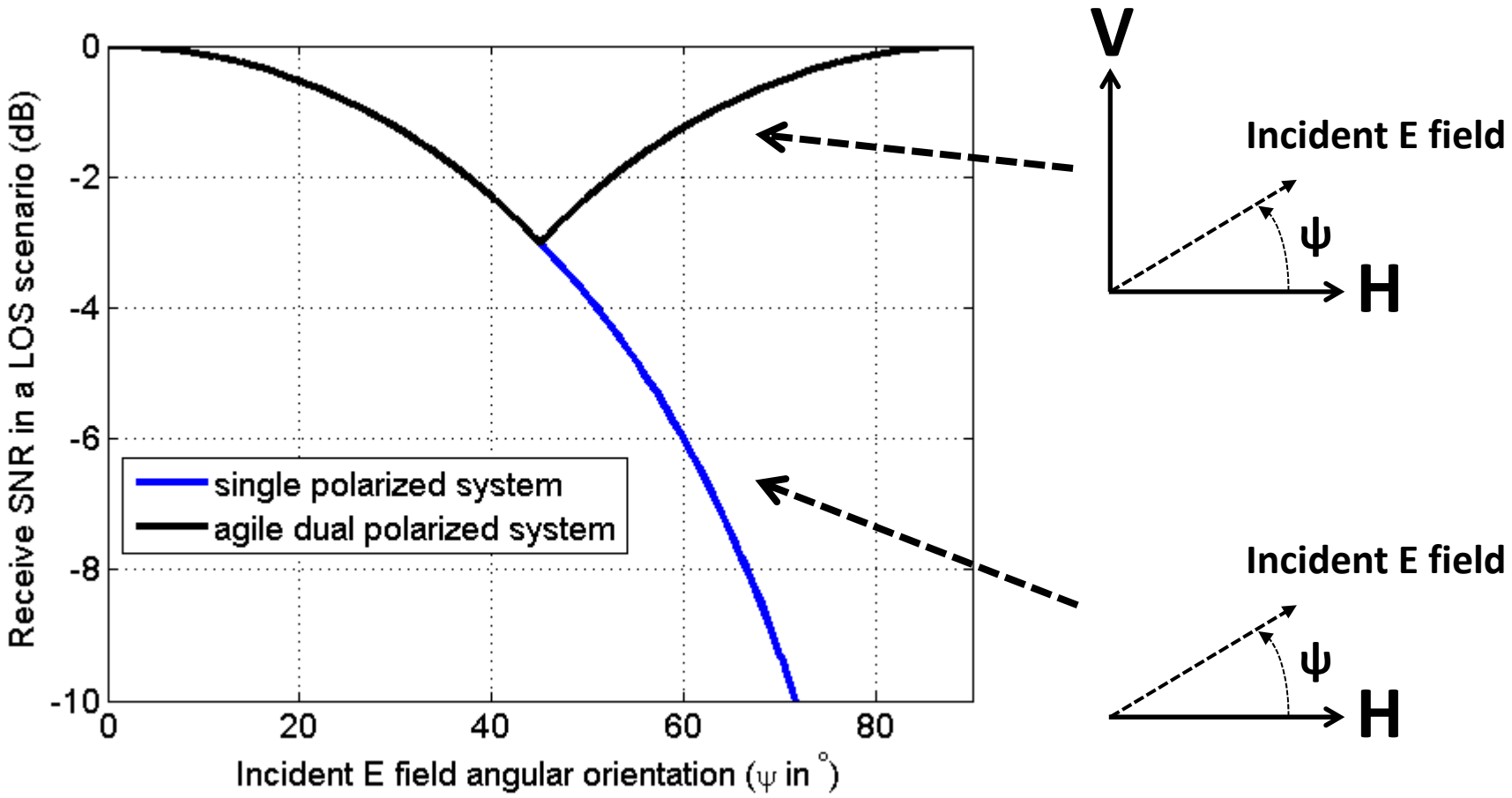
LNA Results

Parameter	Value
NF	<5.5 dB
Ip1dB @ ↑G	-32 dBm
Ip1dB @ ↓G	-22 dBm
Gain	18-25 dB
S11	< -10 dB
Power	35mW
Area	0.15mm^2





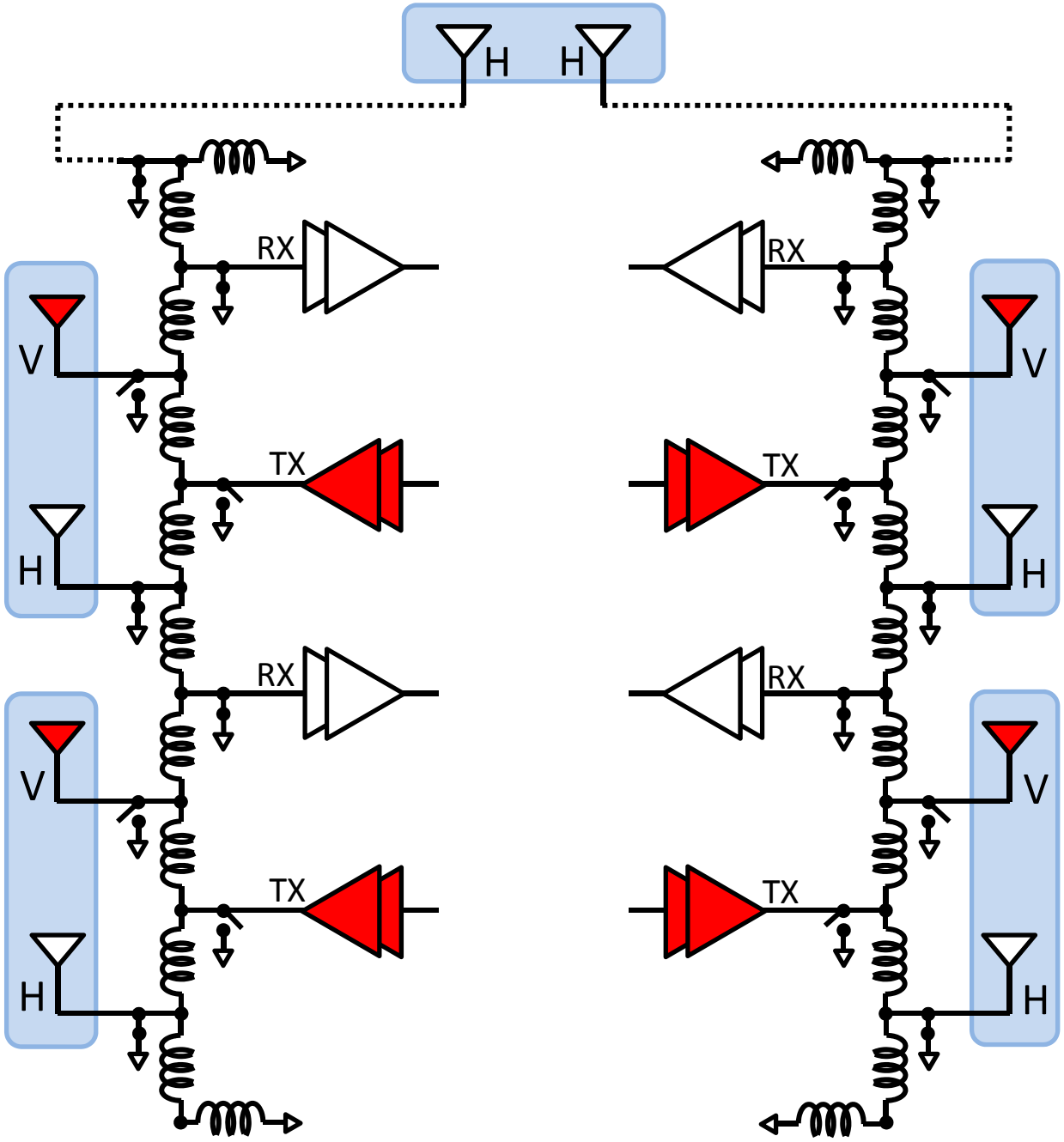
Dual Outputs – Polarization or Spatial Diversity



TX

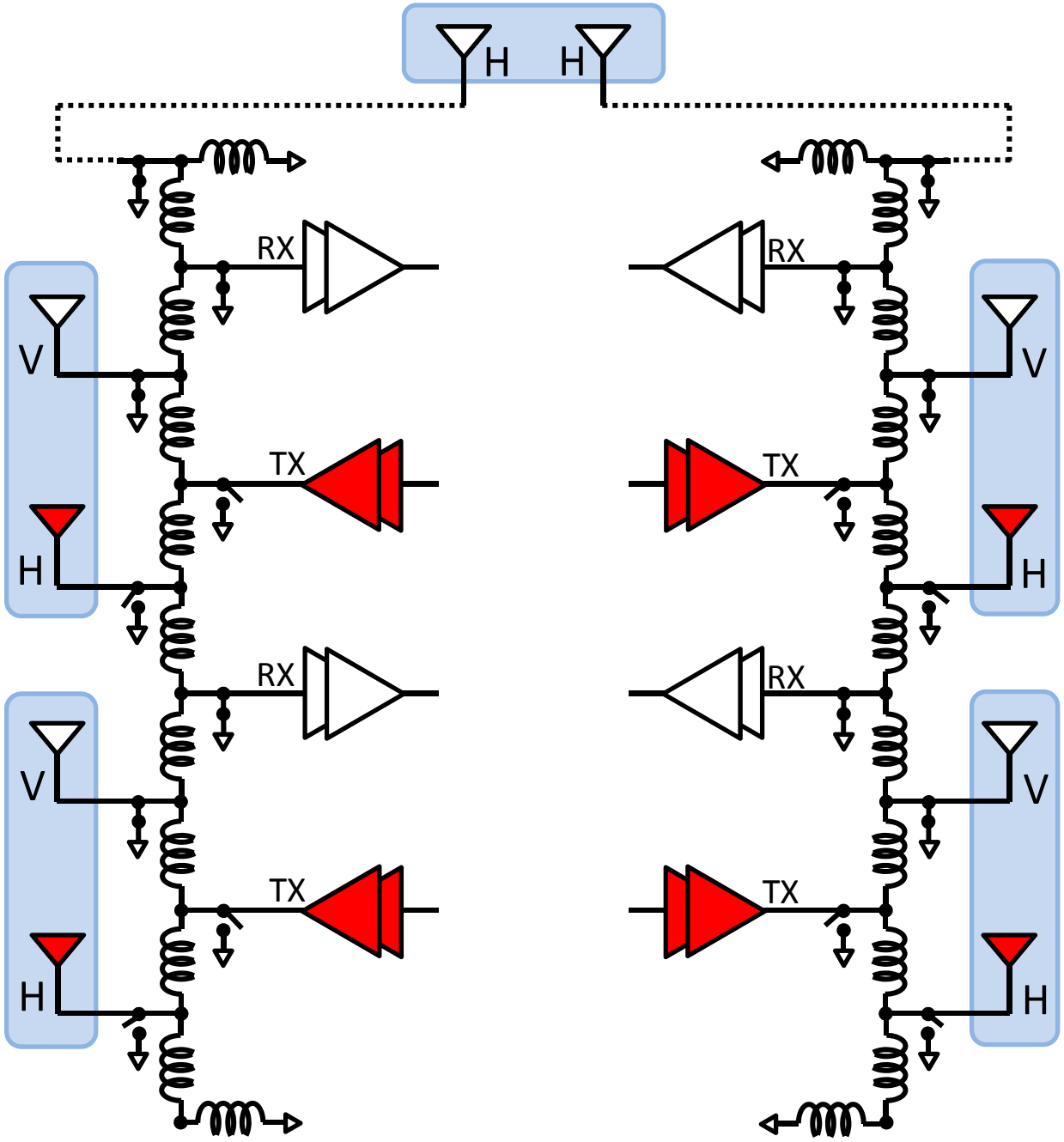
Vertical Polarization

- DPDT
- 2dB SW loss



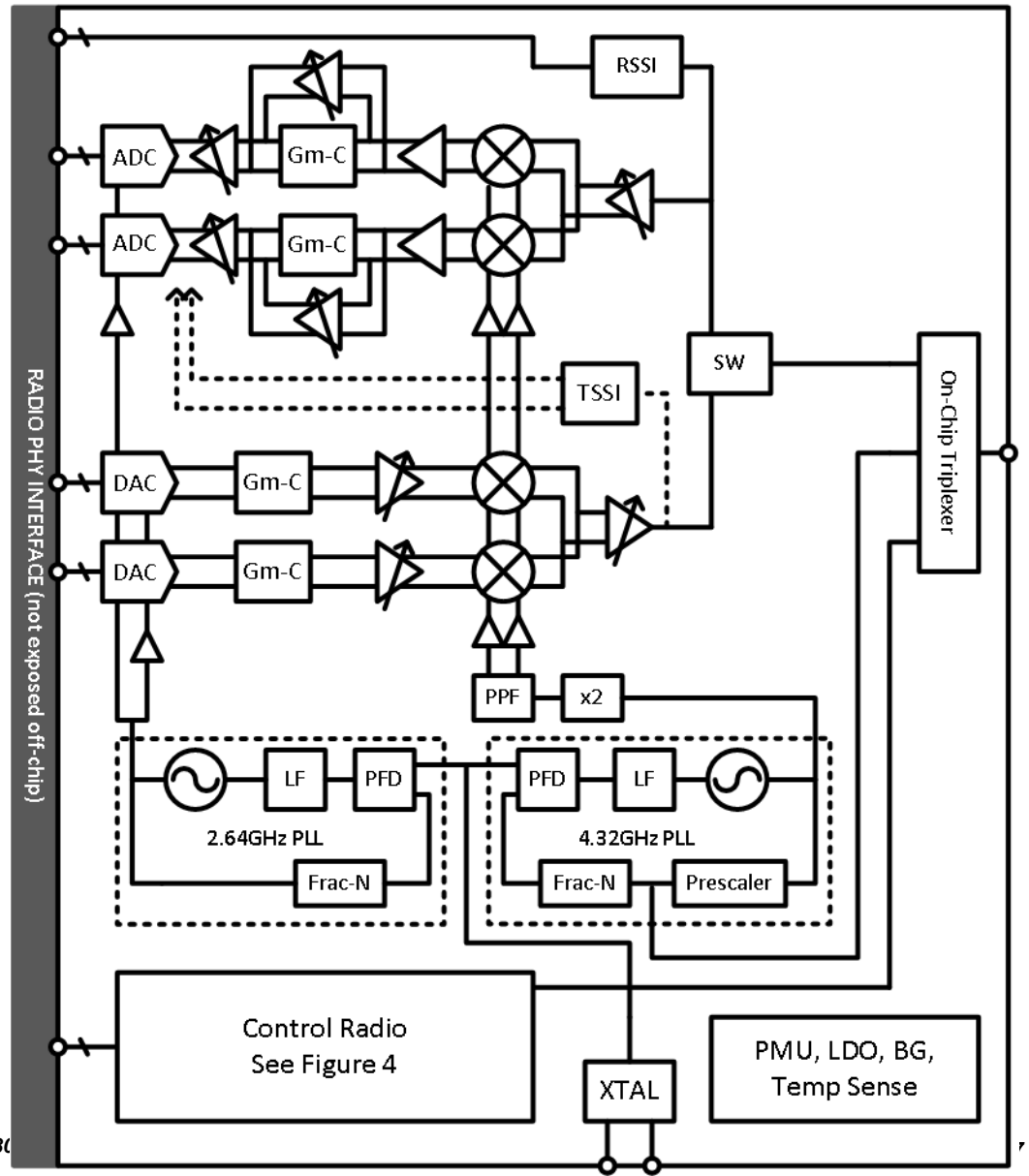
TX

Horizontal Polarization



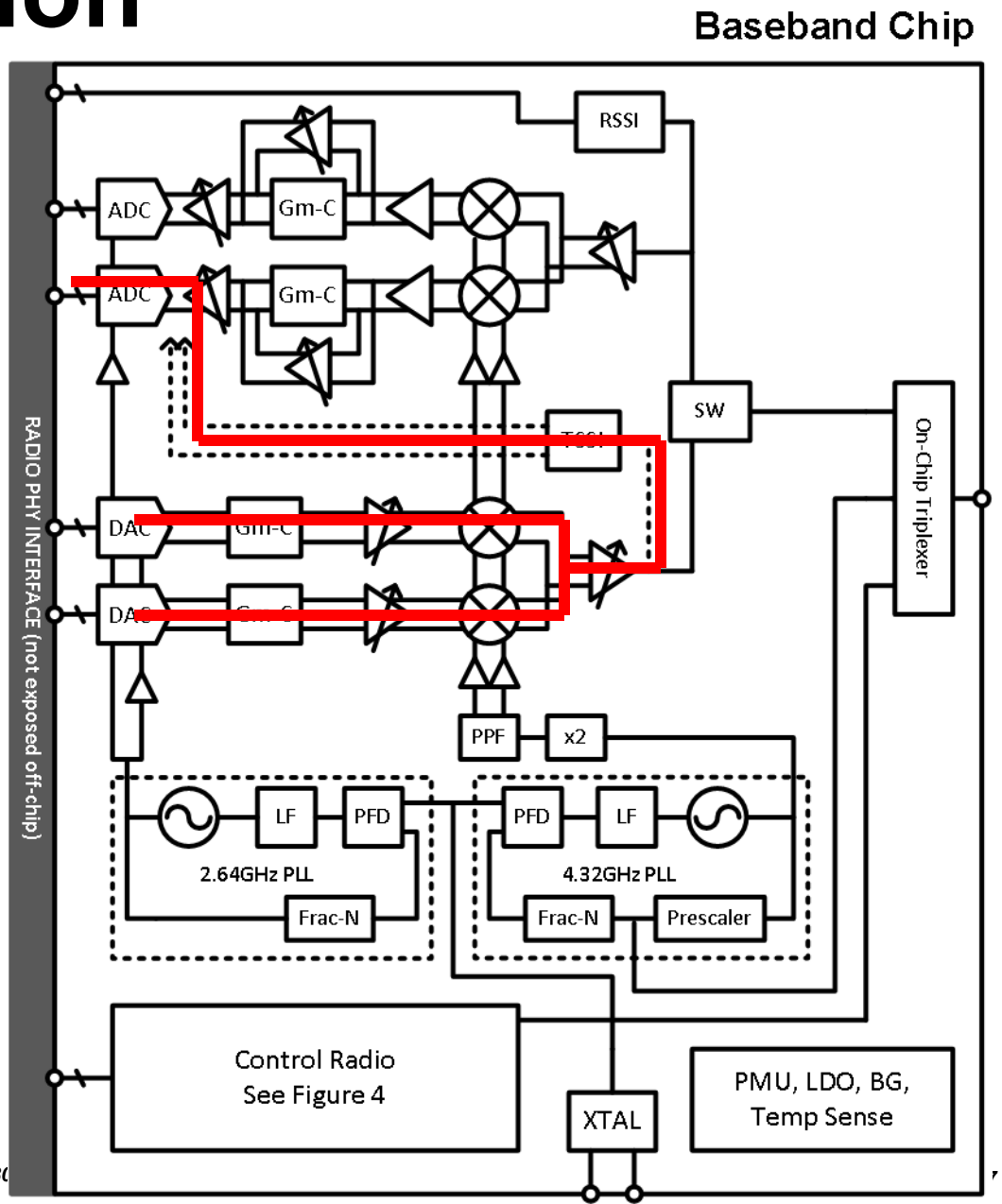
Radio Calibration

- Correct for process variance
- Required for productization
- Useful in self-test



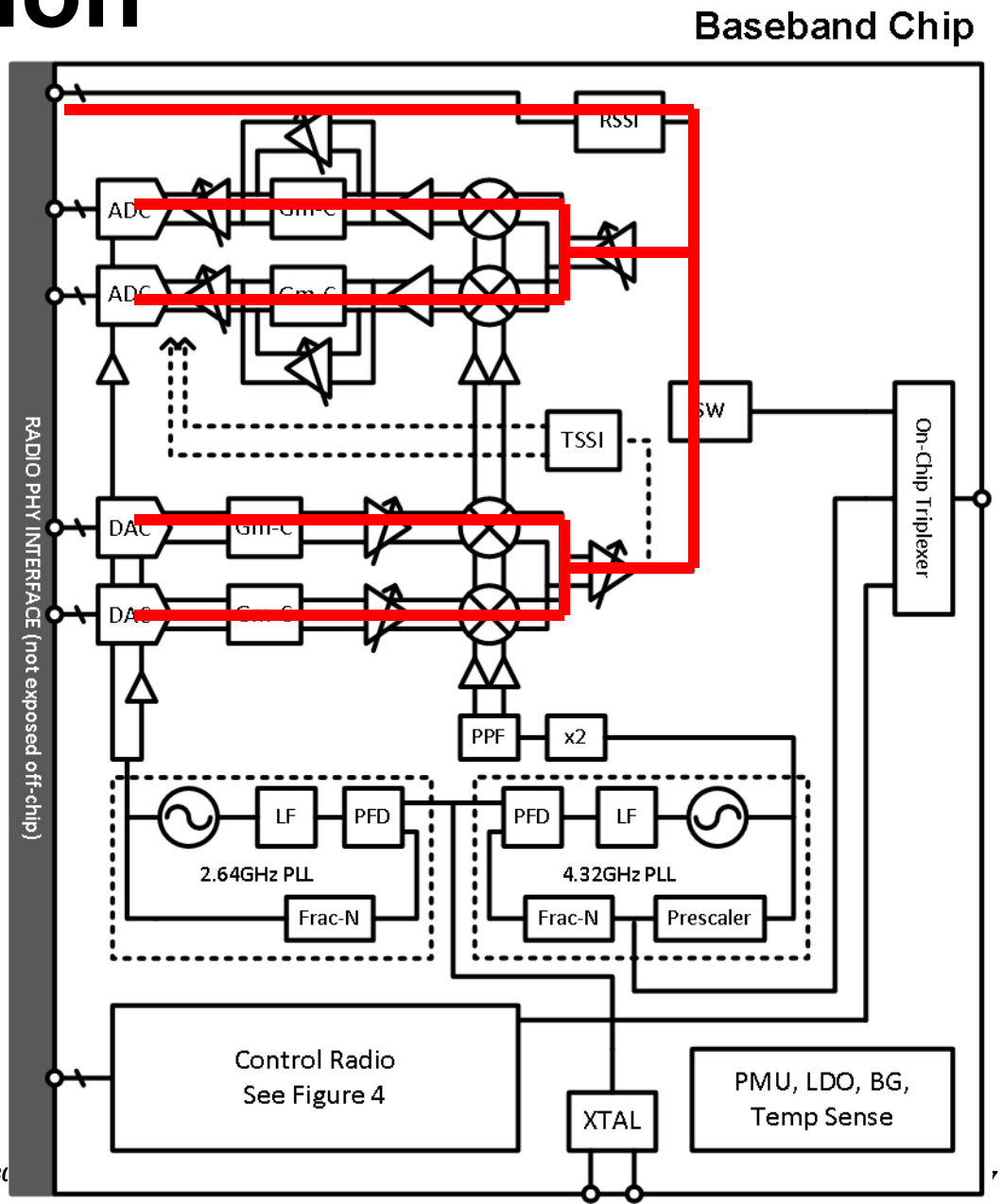
Radio Calibration

- TX IQ



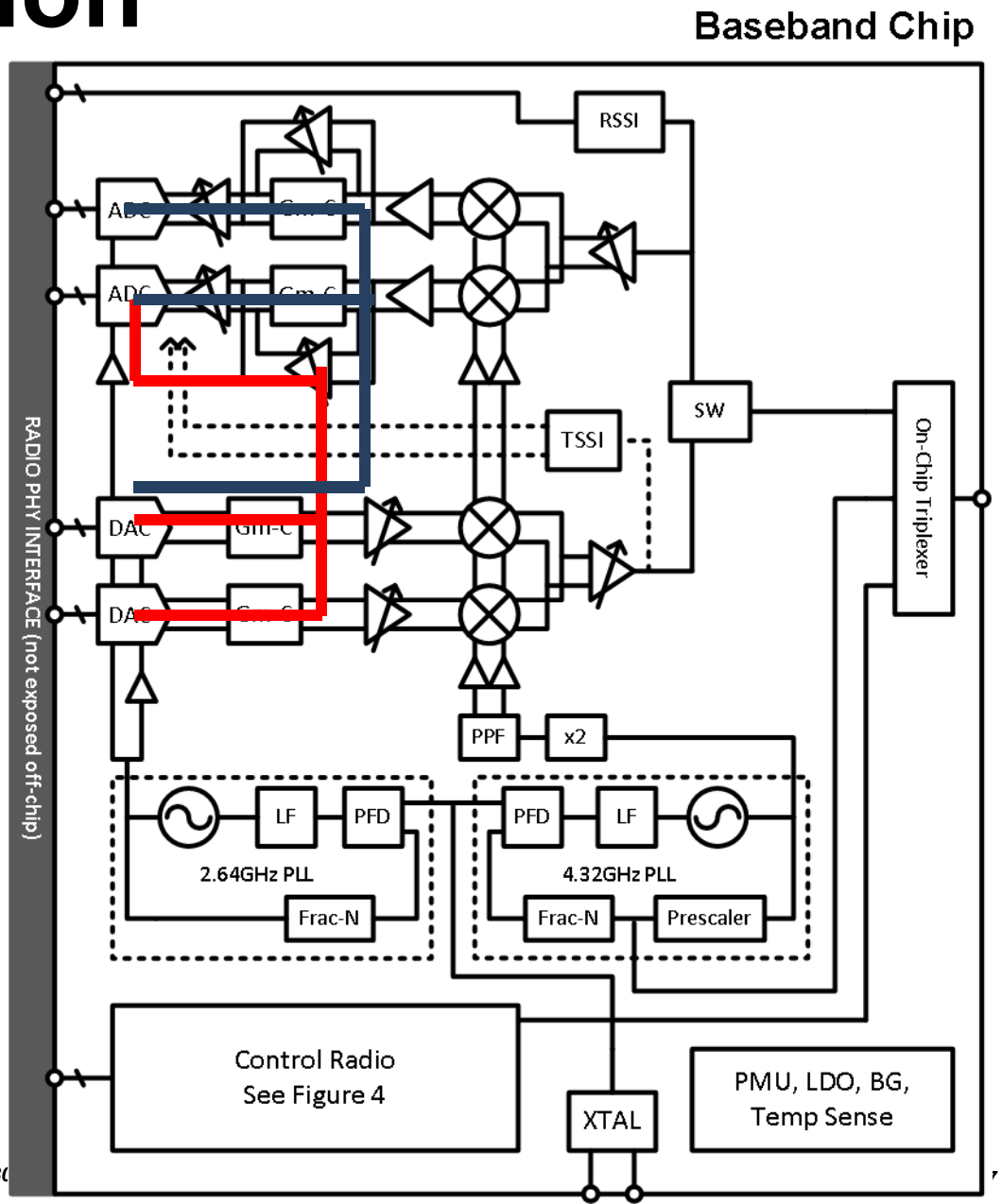
Radio Calibration

- RX IQ
- Gain step



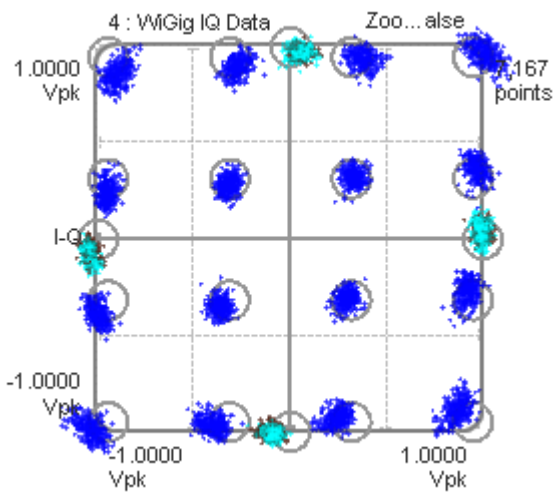
Radio Calibration

- Filters

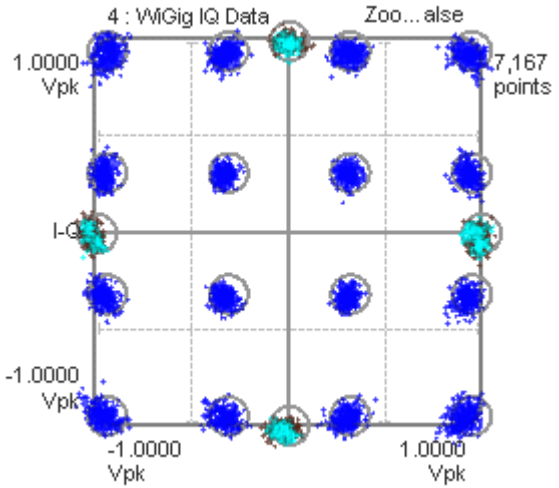


Calibration TX I/Q

- Use TSSI at IF to perform TX I/Q calibration [Cavers97]
- MCS12 – EVM reported at RF output

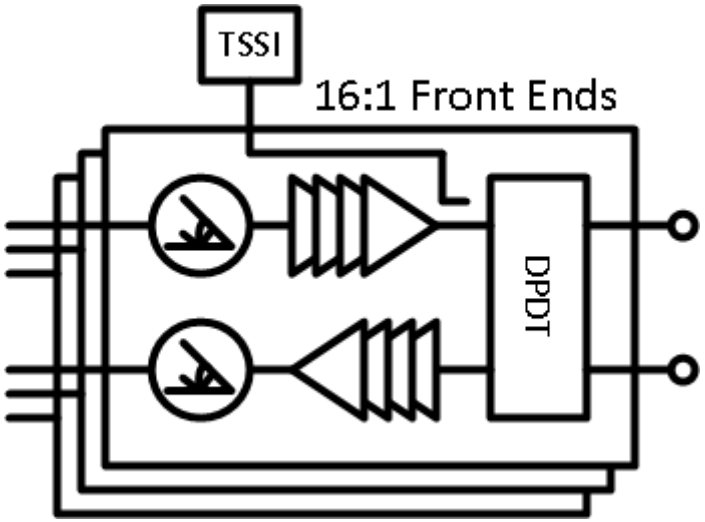


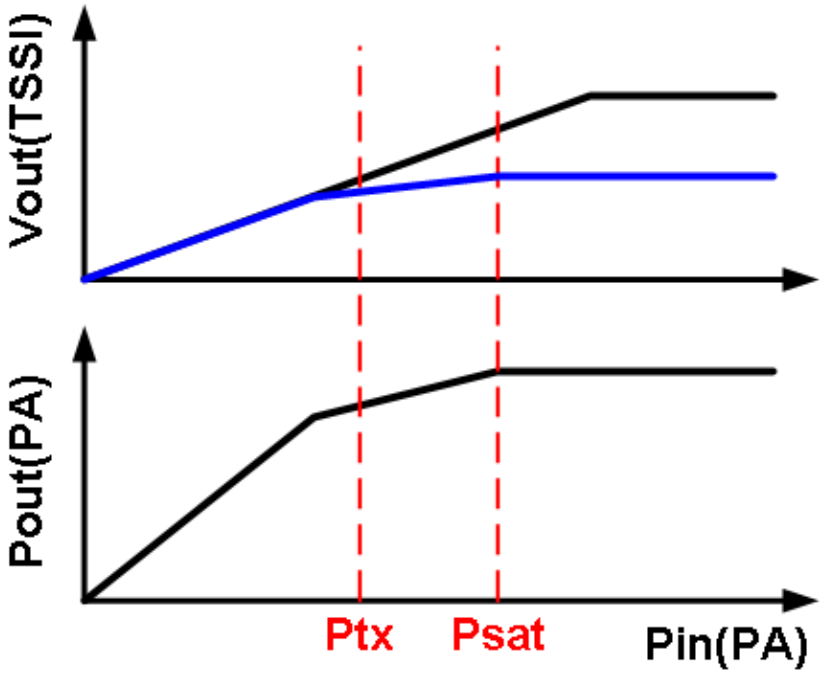
EVM_{RF} -20.9 dB
IQMM amp: 0.24 dB
phase: 7.6 deg



EVM_{RF} -25 dB
IQMM amp: 0.016 dB
phase: 0.29 deg

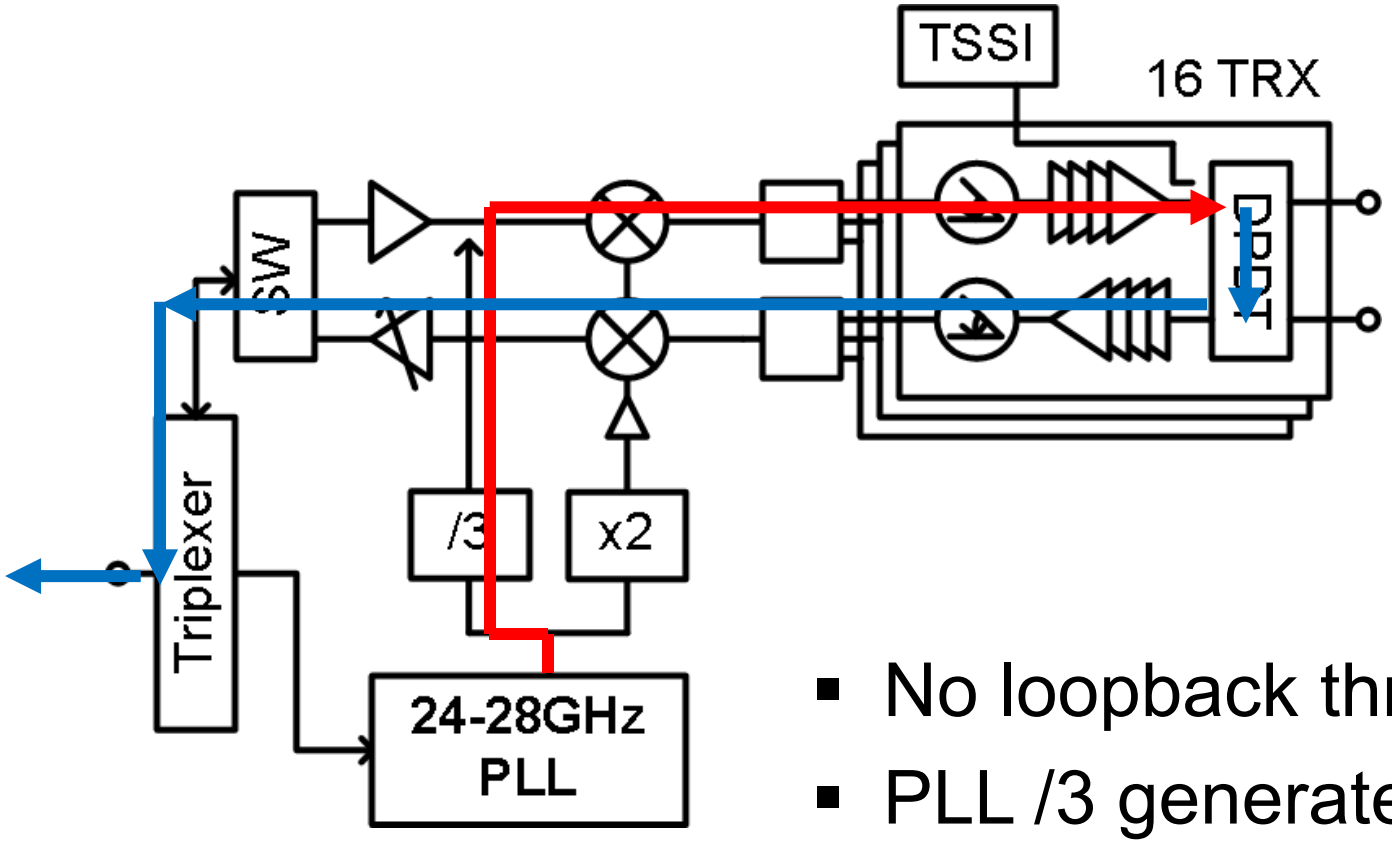
PA (TX Gain) Calibration





- TX gain calibration required
- TSSI at each PA output
- TSSI linear range designed past PA Psat point

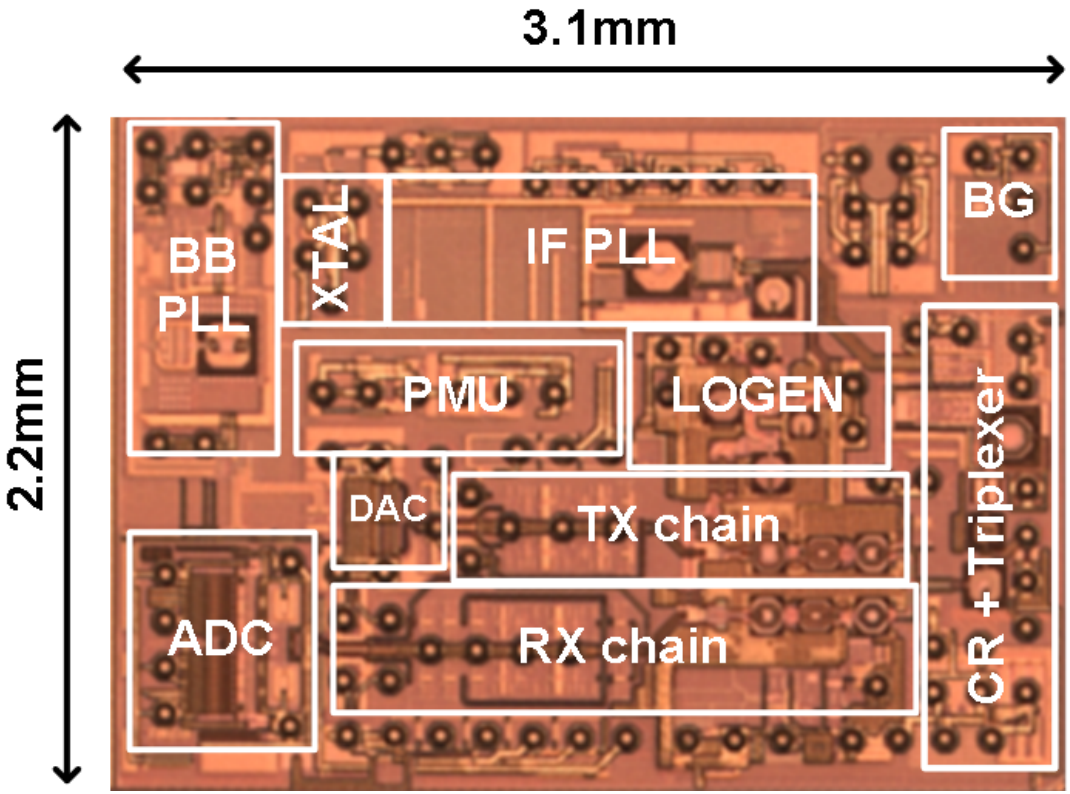
RX Gain Calibration

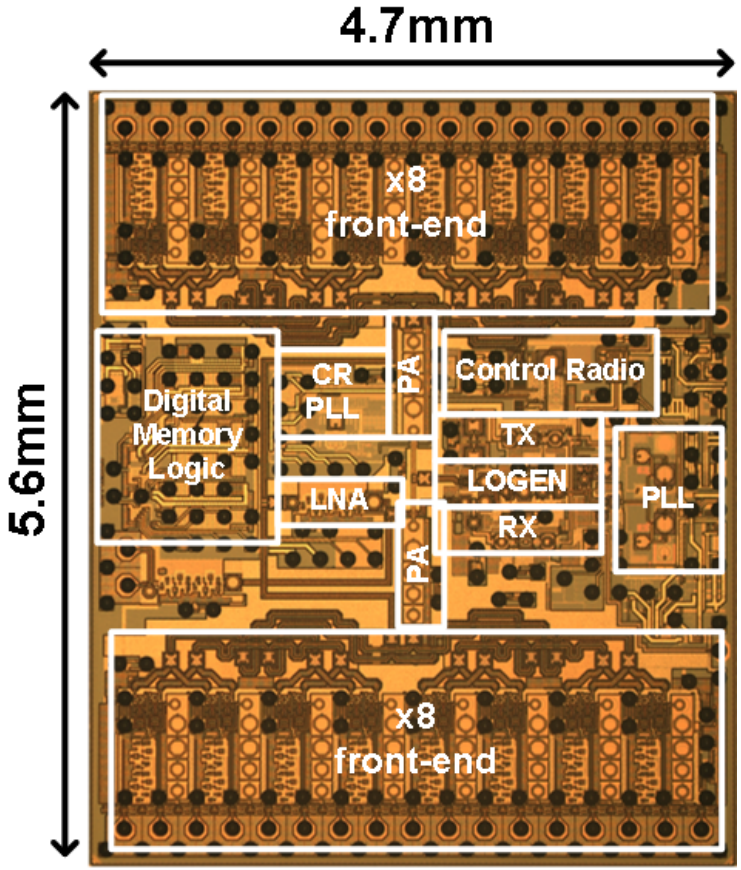


- No loopback through coax
- PLL /3 generates tone
- Gain step, self test

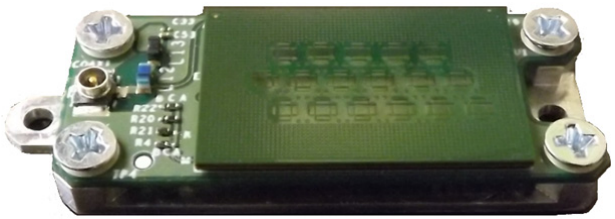
Die Picture

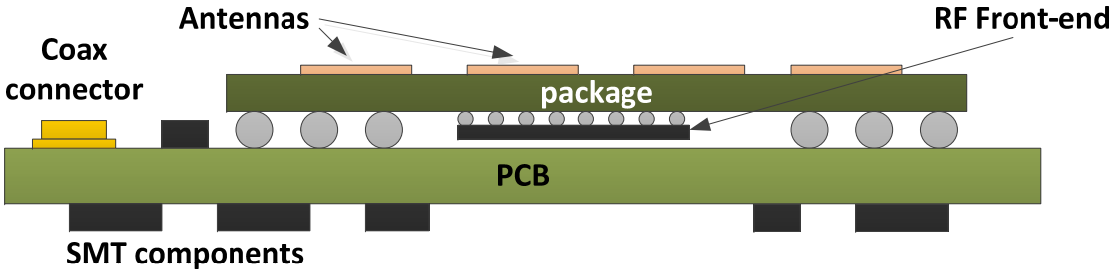
- CMOS 40nm LP
- 6 metals with RDL





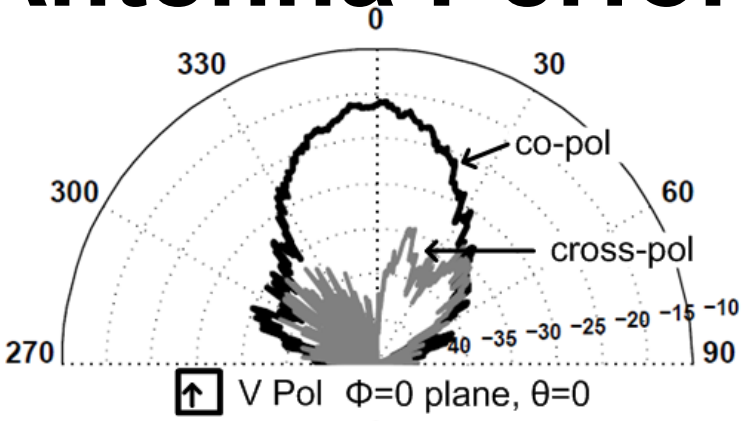
BGA Package



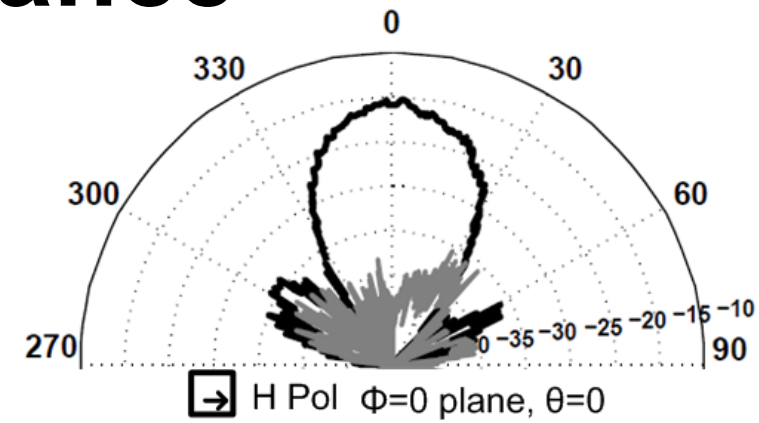


- Low-cost organic laminate.
- 0.2-0.3 dB/mm
- Micro-strip patch CPW-fed antenna.
- Dual linearly polarized antenna with dual-fed for separate V and H access.
- Broadband: 54 to 67GHz.
- Peak gain 4-5dBi.

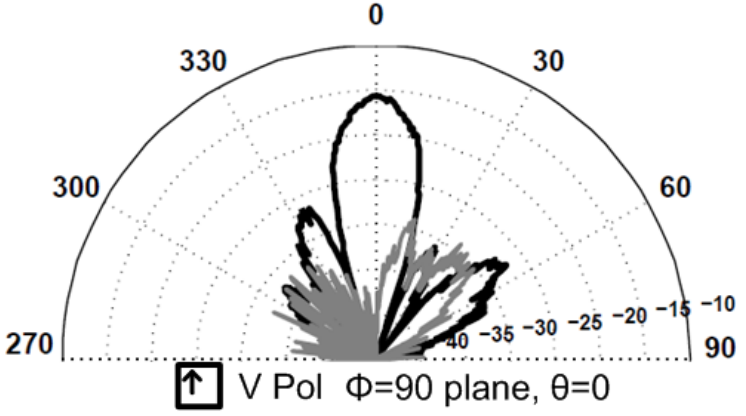
Antenna Performance



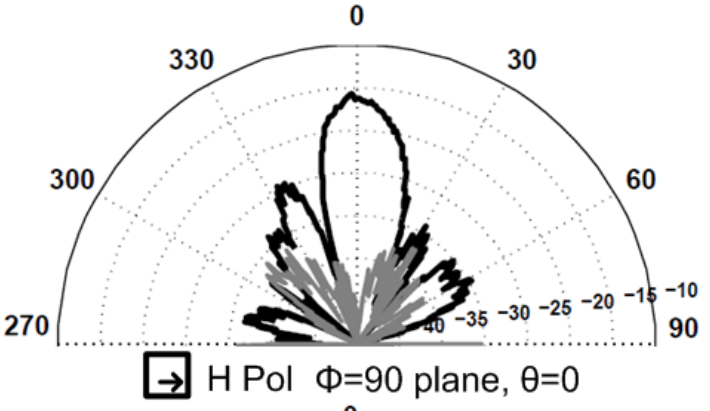
V Pol Φ=0 plane, θ=0



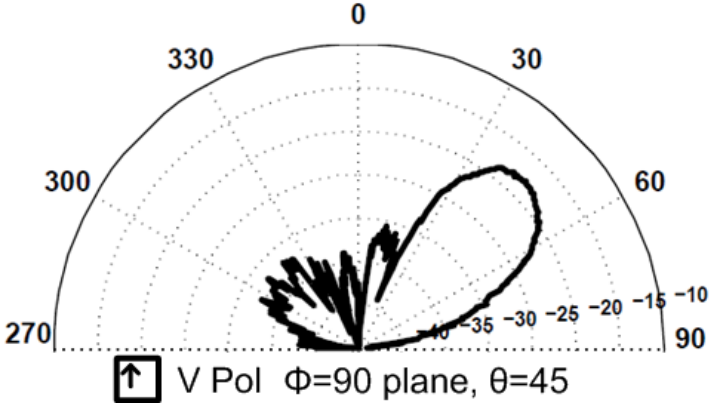
H Pol Φ=0 plane, θ=0



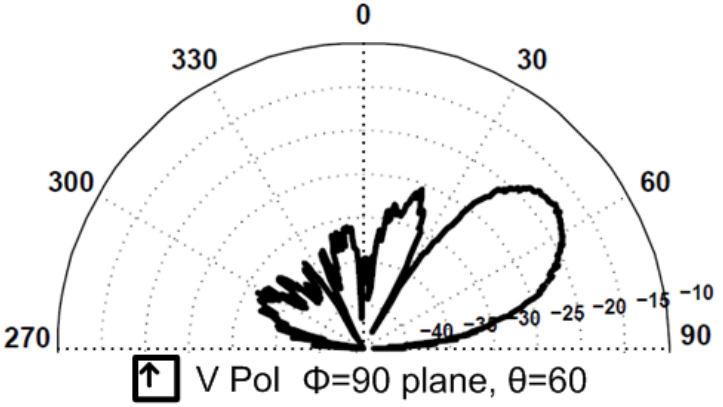
V Pol Φ=90 plane, θ=0



H Pol Φ=90 plane, θ=0



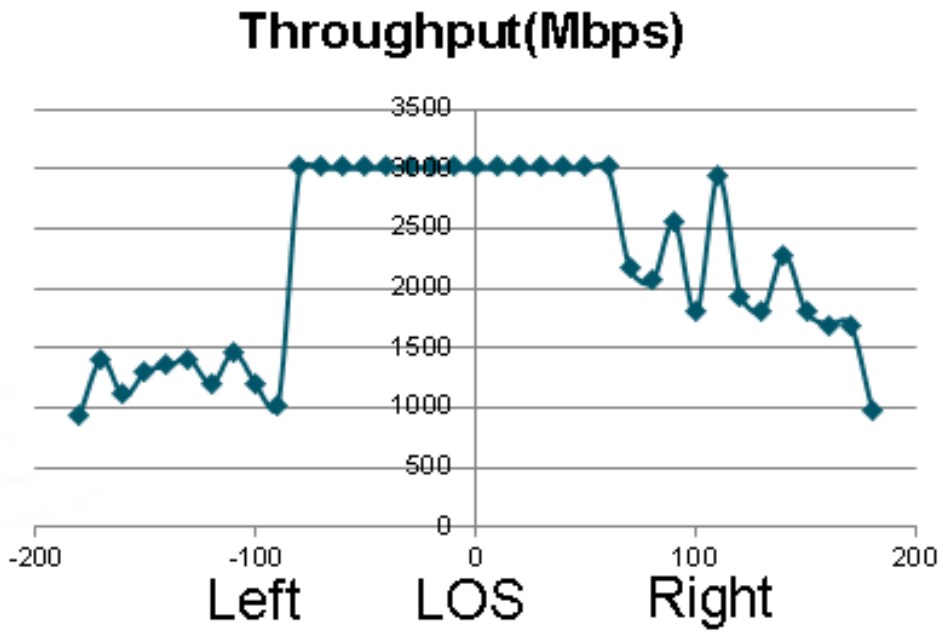
V Pol Φ=90 plane, θ=45

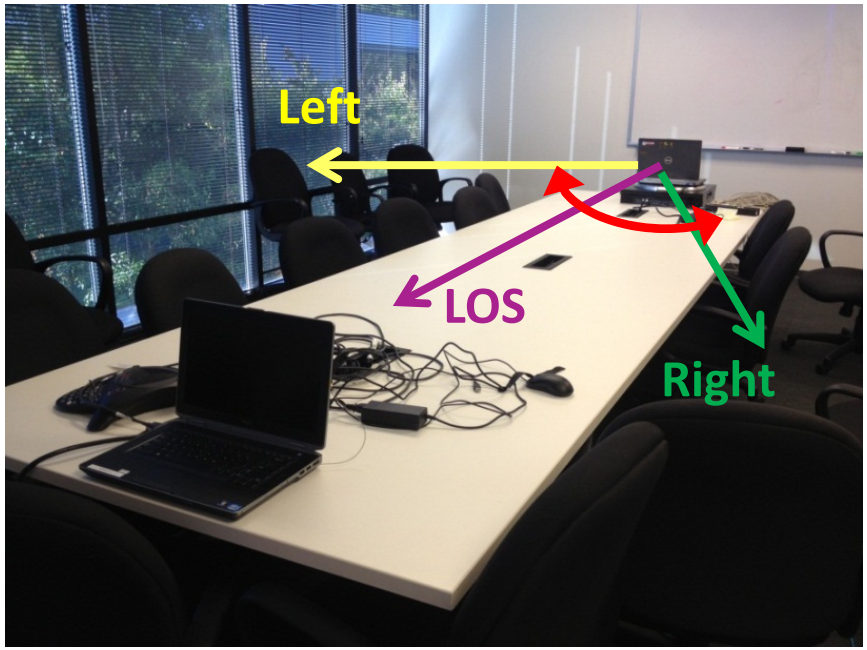


V Pol Φ=90 plane, θ=60

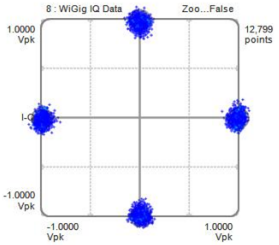
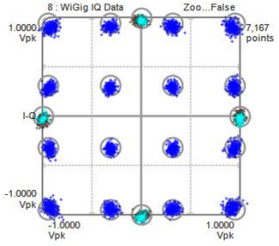
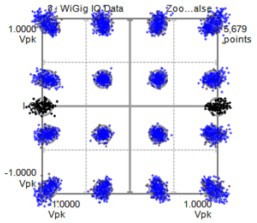
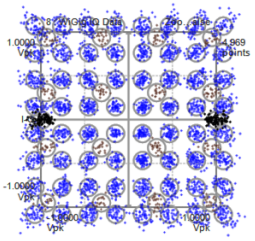
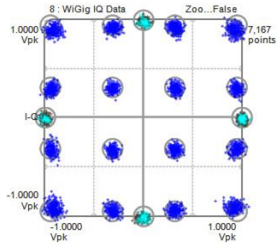
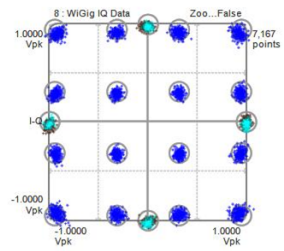
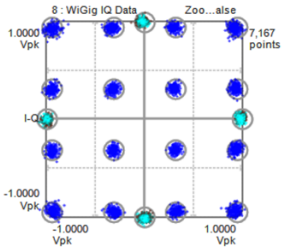
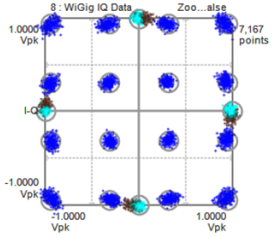
Over the Air Performance

- 3Gbps data rate (3.6Gbps PHY)
- >3Gbps to +/- 90 degrees (NLOS)
- ~1Gbps for multiple reflections





TX EVM

	MCS9 – CH2	MCS12 – CH2	MCS21 – CH2	MCS22 – CH2
Constellation				
Modulation	π/2-QPSK	π/2-16QAM	16QAM	64QAM
SC/OFDM	SC	SC	OFDM	OFDM
EVM meas[1]	-25.2dB	-25.5dB	-22dB	-22dB
EVM meas[2]	-30.3dB	-28.1dB	-27.4dB	-27dB
	MCS12 EVM per channel			
Constellation				
Channel	**1 – 58.32GHz**	**2 – 60.48GHz**	**3 – 62.64GHz**	**4 – 64.8 GHz**
EVM	-24.8dB	-25.5dB	-26.0dB	-24.5dB

[1] EVM measurement with PHY generated data, DAC included

[2] EVM measurement of RF chain only (analog I/Q test-port to 60GHz RF out) after de-embedding of RX test EVM (-33dB)

Comparison

	This work	[1]	[2]	[3]	[4]
Technology	40nm LP	40nm / 90nm	40nm	65nm	90nm
Interface	Single Coax	Analog I/Q	Analog I/Q	Analog I/Q	IF
Supported Channels	**4**	4	3	2	2
Integration	**PCIe, PHY, MAC, RF**	USB3, PHY, MAC, RF	RF only	RF only	IF to RF only
Total Radio Area	33	13.5	12.5	72.68	29[1]
Architecture	16TX 16+1RX	1TX 1RX	4TX 4RX	32TX 8 RX	32TX 32+1RX
Single wire interface	**Yes**	No	No	No	No
Polarization diversity	**Yes**	No	No	No	No
EIRP	24 dBm @ -23dB EVM	8.5 dBm @ -22dB EVM	22.5 dBm	28 dBm @ -19dB EVM	29 dBm @ -19dB EVM
TX EVM	**-23 dB** @ EIRP	-22 dB @ EIRP		-19 dB @ EIRP	-19 dB @ EIRP
TX+RX EVM	**-19.5dB**		-15.2dB		
RX NF	<10dB (2dB sw)	7.1dB	8.7dB	10dB	<10dB
Radio RX die power	960 mW	274 mW	496 mW		850 mW[1]
Radio TX die power	1190 mW	347 mW	584 mW	1800 mW	1200 mW[1]
Radio mm^2 / element	1.00	not phased array	1.56	1.82	0.45[1]
Link distance (PHY rate)	**4.6Gbps @ 10m** 3.0Gbps @ 20m	1.8Gbps @ 0.8m	4.6Gbps @ 0.7m 2.3Gbps @ 3.6m	3.8 Gbps @ 50m	
Notes	[1] IF to RF chain only				

Summary

- First chipset with PCI-e/MAC/PHY/RF, control radio and polarization diversity
  - 16TX/RX antenna array
  - Solves placement problem
- System tolerant to PVT
  - Built-in calibration and self-test
- Performance
  - 64-QAM TX
  - Best TX+RX 16-QAM EVM
  - 4.6Gbps over 10m LOS

References

[1] T. Tsukizawa, et al., “A Fully Integrated 60GHz CMOS Transceiver Chipset Based on WiGig/IEEE802.11ad with Built-In Self Calibration for Mobile Applications” ISSCC Dig. Tech. Papers, pp. 230-231, Feb., 2013.

[2] V. Vidojkovic, et al., “A Low-Power Radio Chipset in 40nm LP CMOS with Beamforming for 60GHz High-Data-Rate Wireless Communication” ISSCC Dig. Tech. Papers, pp. 236-237, Feb., 2013.

[3] S. Emami, et al., “A 60GHz CMOS Phased-Array Transceiver Pair for Multi-Gb/s Wireless Communications” ISSCC Dig. Tech. Papers, pp. 164-165, Feb., 2011.

[4] E. Cohen, et al., “A CMOS Bidirectional 32-element Phased-Array Transceiver at 60GHz with LTCC Antenna” Radio Frequency Integrated Circuits Symposium (RFIC), pp.439,442, Jun., 2012.

A 64-QAM 60GHz CMOS Transceiver with 4-Channel Bonding

Kenichi Okada, Ryo Minami, Yuuki Tsukui,
Seitaro Kawai, Yuuki Seo, Shinji Sato,
Satoshi Kondo, Tomohiro Ueno, Yasuaki Takeuchi,
Tatsuya Yamaguchi, Ahmed Musa, Rui Wu,
Masaya Miyahara, and Akira Matsuzawa

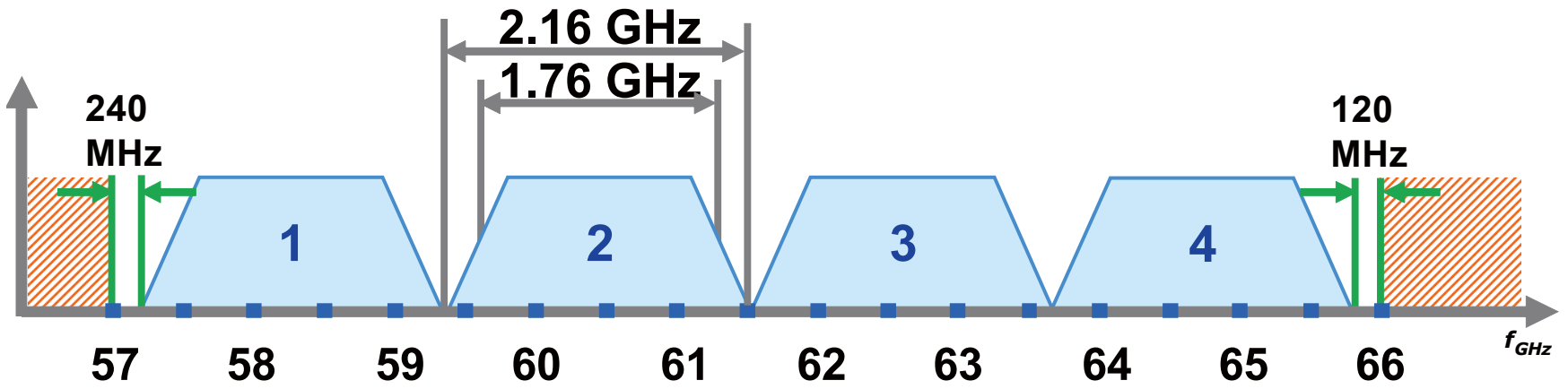
Tokyo Institute of Technology, Japan

Outline

- Motivation
- Transmitter
  - Mixer-first transmitter
- Receiver
  - Open-loop FVF-based amp.
- Measurement and Comparison
- Conclusion

60GHz-Band Capability

- QPSK → 3.52Gbps/ch
- 16QAM → 7.04Gbps/ch
- 64QAM → 10.56Gbps/ch (not reported yet)
- 16QAM
  - 2-ch bonding → 14.08Gbps
  - 3-ch bonding → 21.12Gbps (not reported yet)
  - 4-ch bonding → 28.16Gbps (not reported yet)



from IEEE802.11ad/WiGig

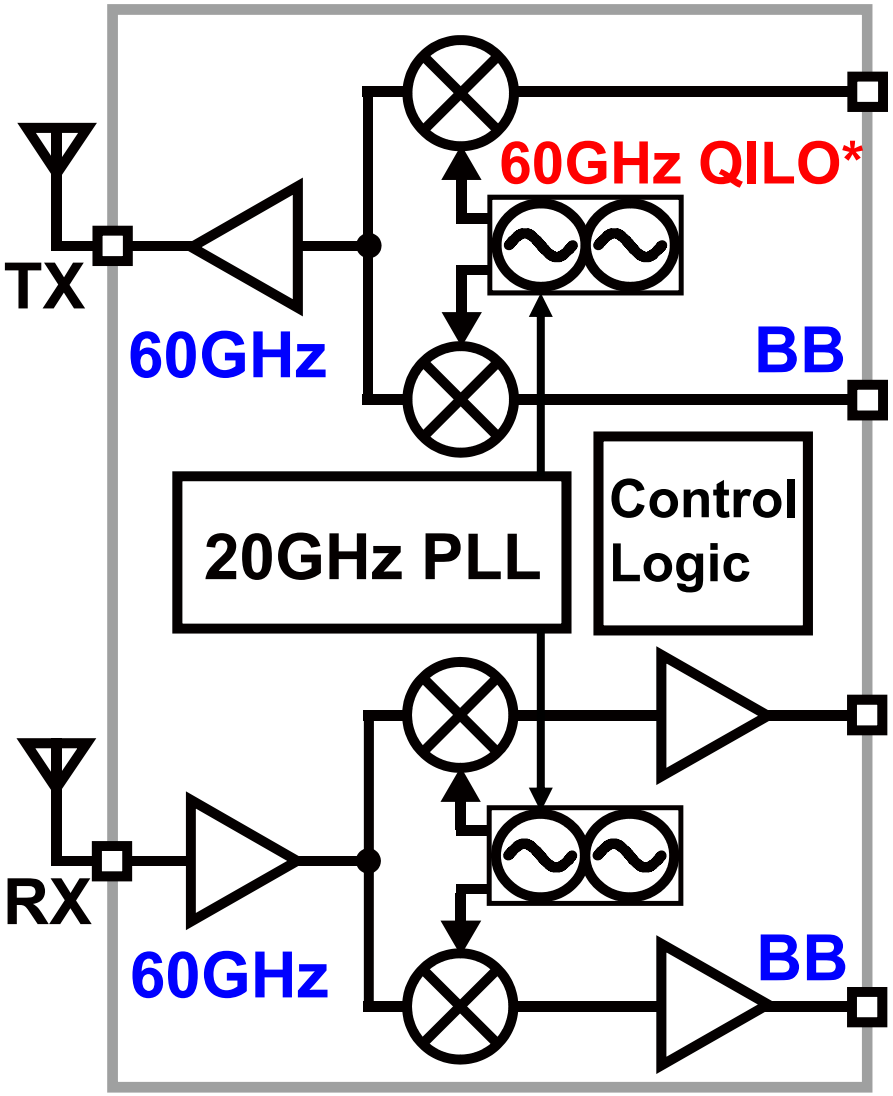
Design Considerations

- Wideband gain characteristics
  - RF: 57-66GHz
  - BB: 1.2GHz(1ch), 5GHz(4-ch bonding)
- Wide dynamic range
  - Linearity & Sensitivity
  - RX SNDR >40dB
- Low phase noise (performance limiter)*
  - -96dBc/Hz@1MHz (64QAM)
- I/Q mismatch & LO leakage**
  - Image rejection ratio <-40dBc

*K. Okada, *et al.*, JSSC 2013

**S. Kawai, *et al.*, RFIC 2013

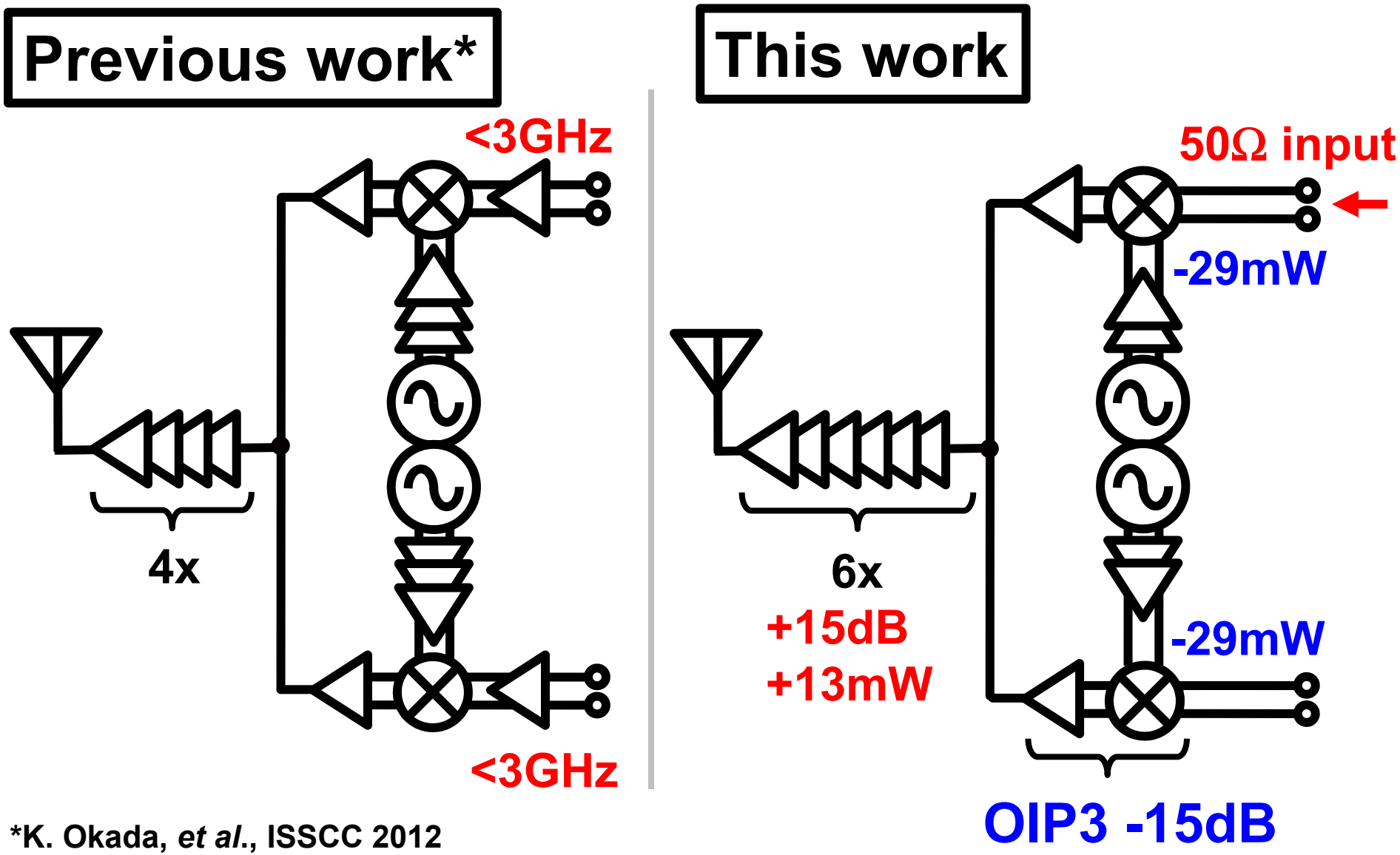
Block Diagram



- Direct-conversion
- TX
  - Mixer-first topology
- RX
  - FVF BB amp.
  - Current-bleeding mixer
- LO
  - Injection-lock
  - 60GHz QILO* +20GHz PLL

*K. Okada, *et al.*, ISSCC 2011

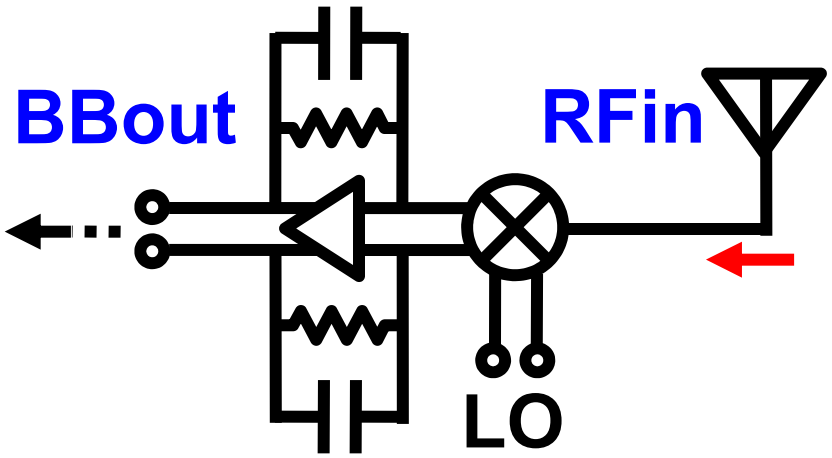
TX Design Considerations

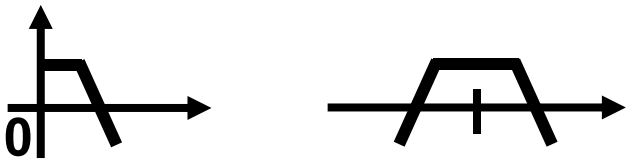


*K. Okada, *et al.*, ISSCC 2012

Mixer-First Transmitter

Mixer-first receiver*, **

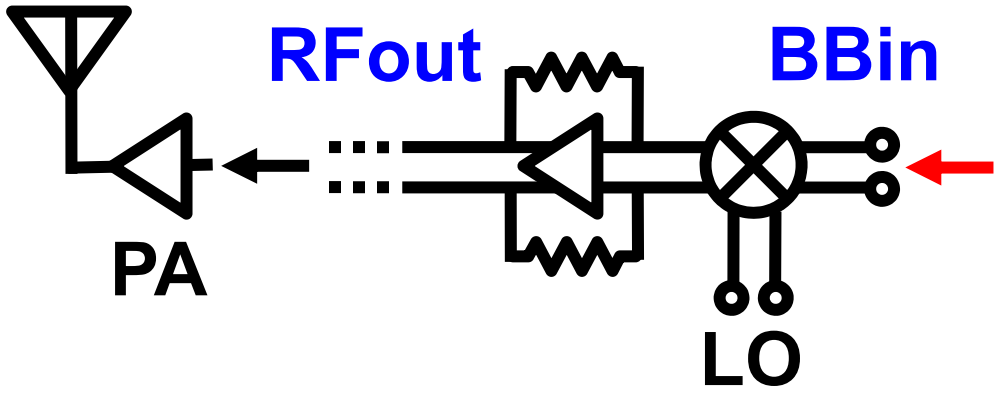


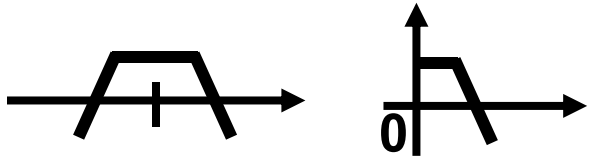


10MHz up-converted** → 2GHz (20MHz-BW)

Mixer-first transmitter

This work



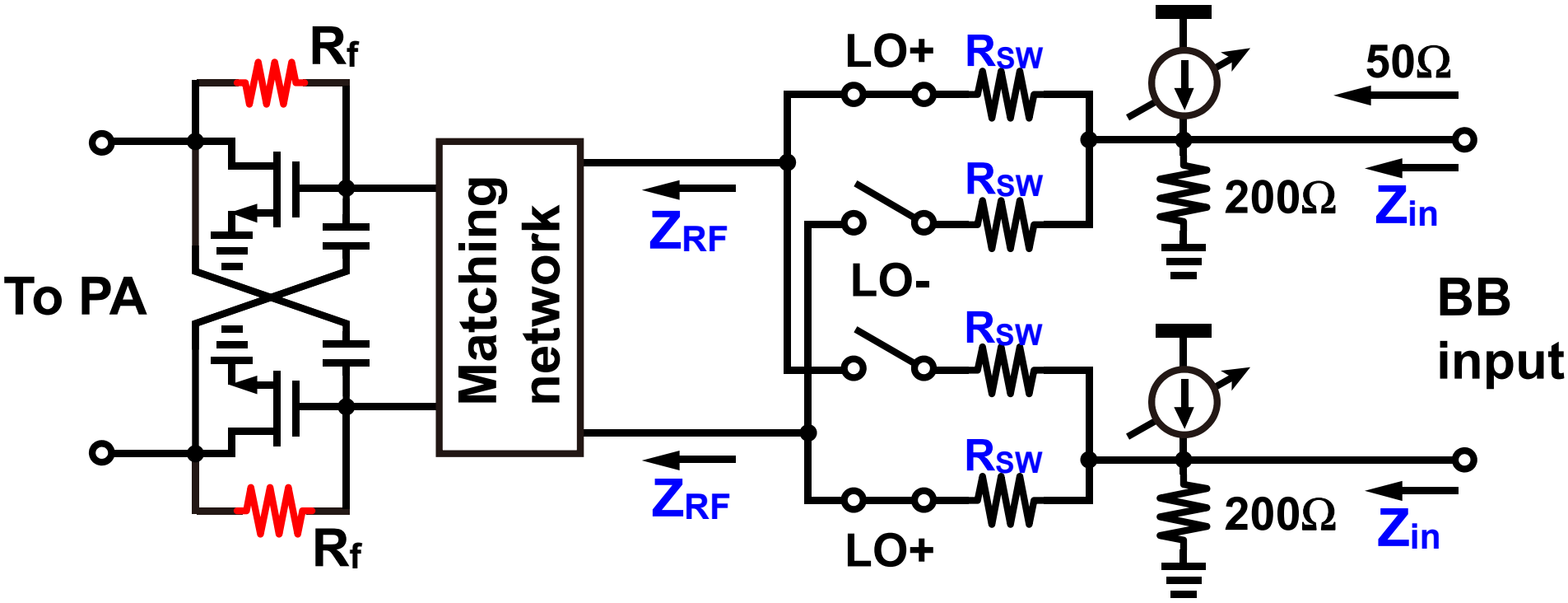


57-66GHz (9GHz-BW) → 4.5GHz

down-converted even for Z_{in}

*M. Soer, *et al.*, ISSCC 2009 **C. Andrews, *et al.*, ISSCC 2010

Input Impedance and Leakage Cancel



$$Z_{\mathrm{in}}(\omega_{\mathrm{BB}}) = 200\Omega /\!\!/ \left[R_{\mathrm{sw}} + \frac{4}{\pi^2}\{Z_{\mathrm{RF}}(\omega_{\mathrm{BB}} + \omega_{\mathrm{LO}}) + Z_{\mathrm{RF}}(\omega_{\mathrm{BB}} - \omega_{\mathrm{LO}})\} \right]$$

Wideband Z_{RF} is realized by R_f-feedback.

*C. Andrews, *et al.*, ISSCC 2010

TX Measurement Result

Lower-side-band gain including RF path

LO=61.56GHz

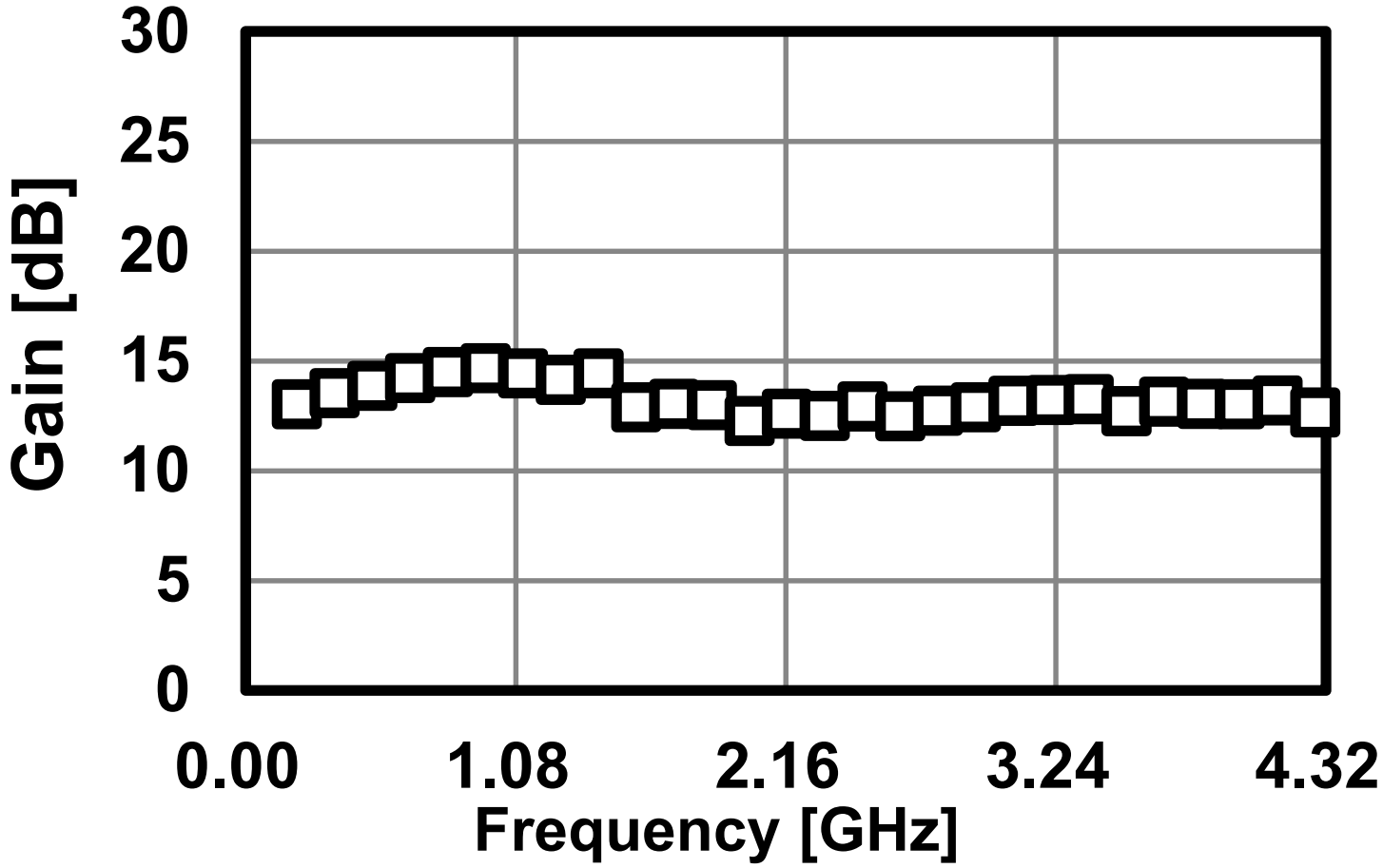
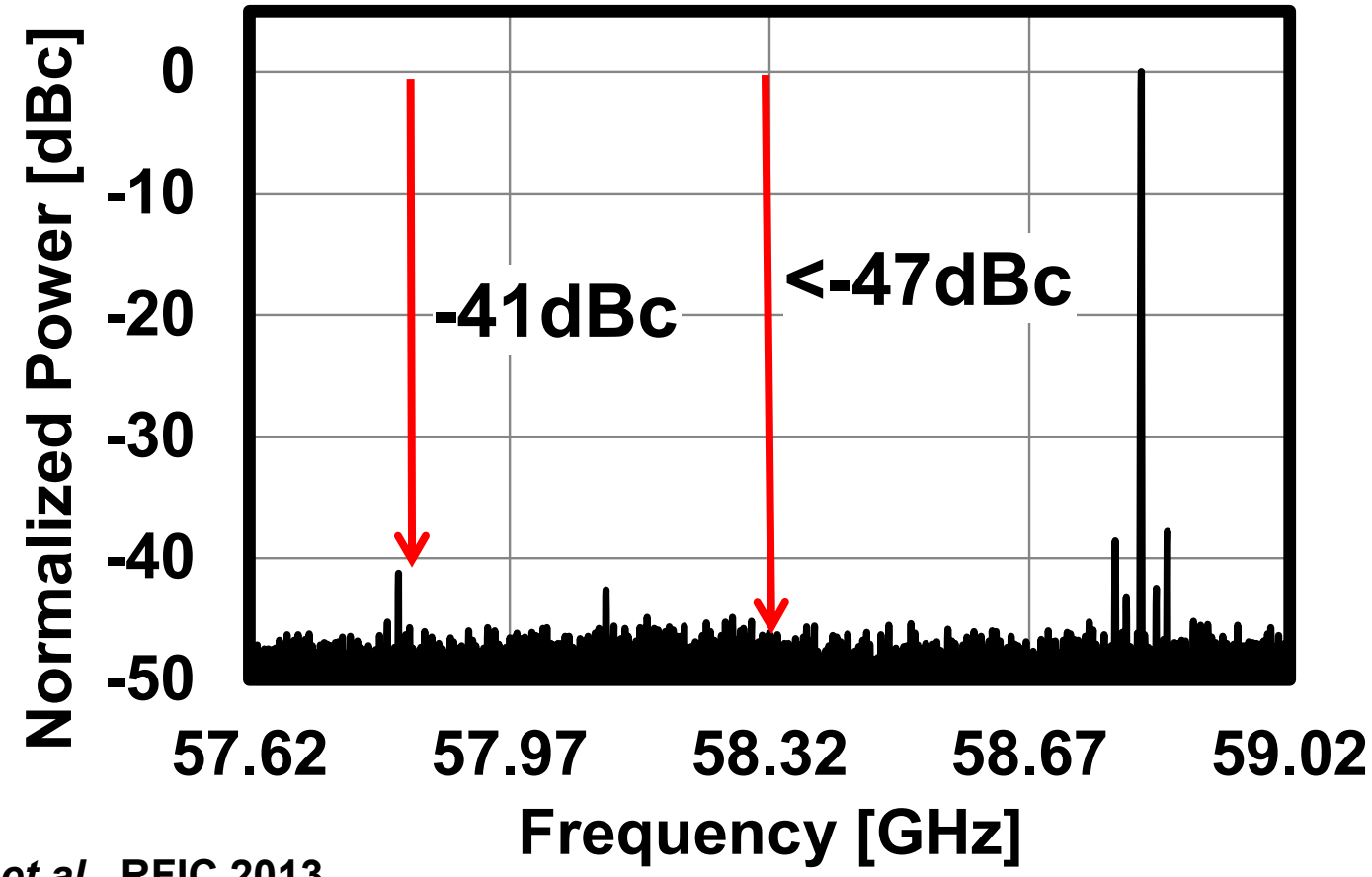


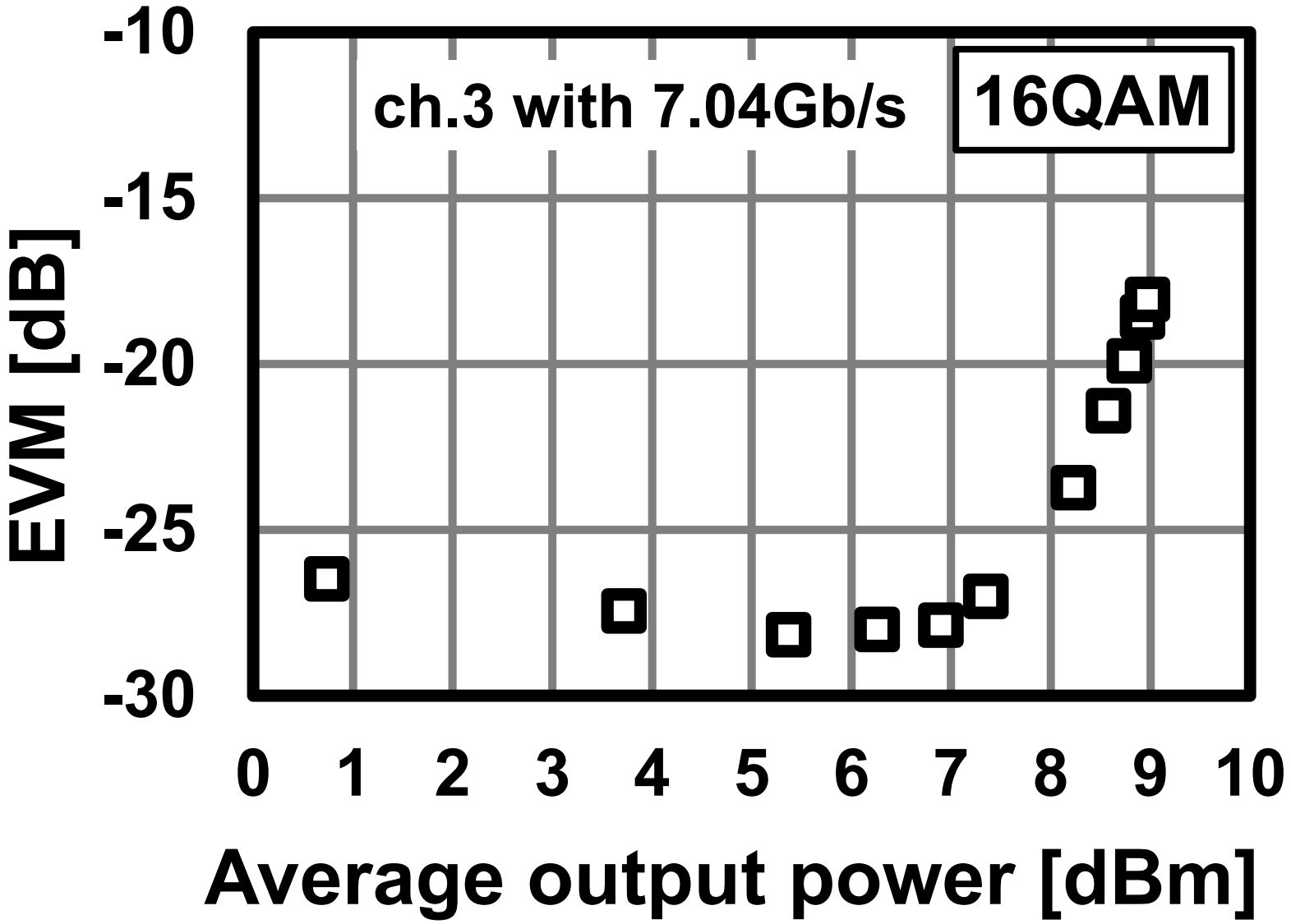
Image Rejection & LO Leakage

I/Q mismatch calibration* is applied.
RF VGA & QILO phase adjustment

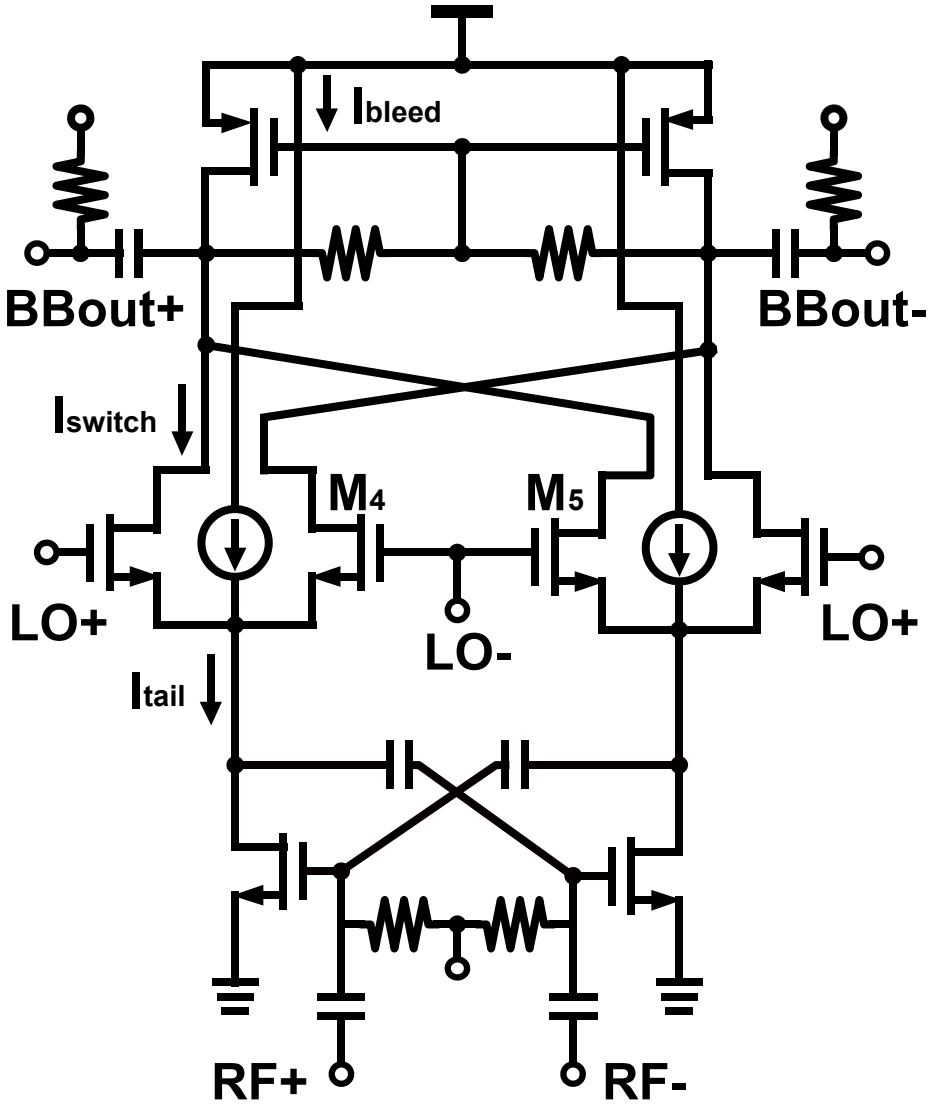


*S. Kawai, *et al.*, RFIC 2013

TX EVM Measurement



RX Mixer



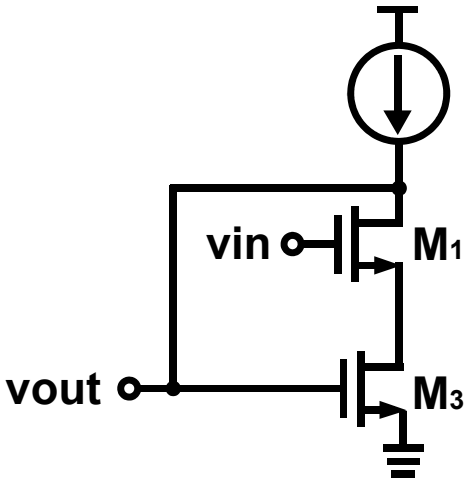
- Current-bleeding to reduce LO power
- CCC at RF input

- Pdc: 11mW
- CG: -7dB
- f_{low}: 0.27MHz
- f_{high}: >4GHz

RX Baseband Amplifier

- Wide bandwidth (>5GHz)
- High gain and high linearity
- Low power consumption

⇨ Open-loop FVF-based amplifier

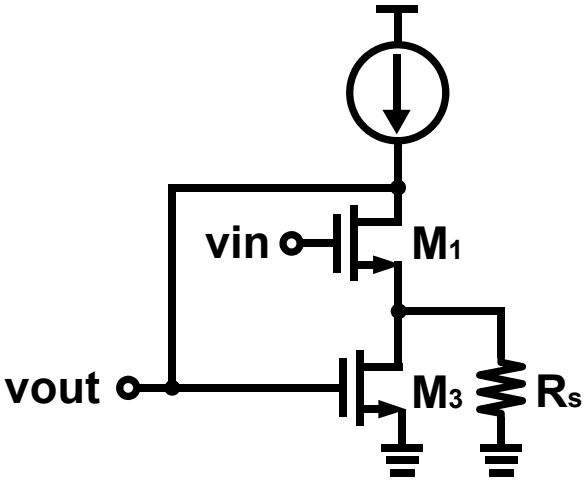


$$A_V \cong -\frac{g_{ds3}}{g_{m3}}$$

Flipped Voltage Follower* (FVF)

*R. Carvajal, *et al.*, TCAS-I 2005

RX Baseband Amplifier (*Cont.*)

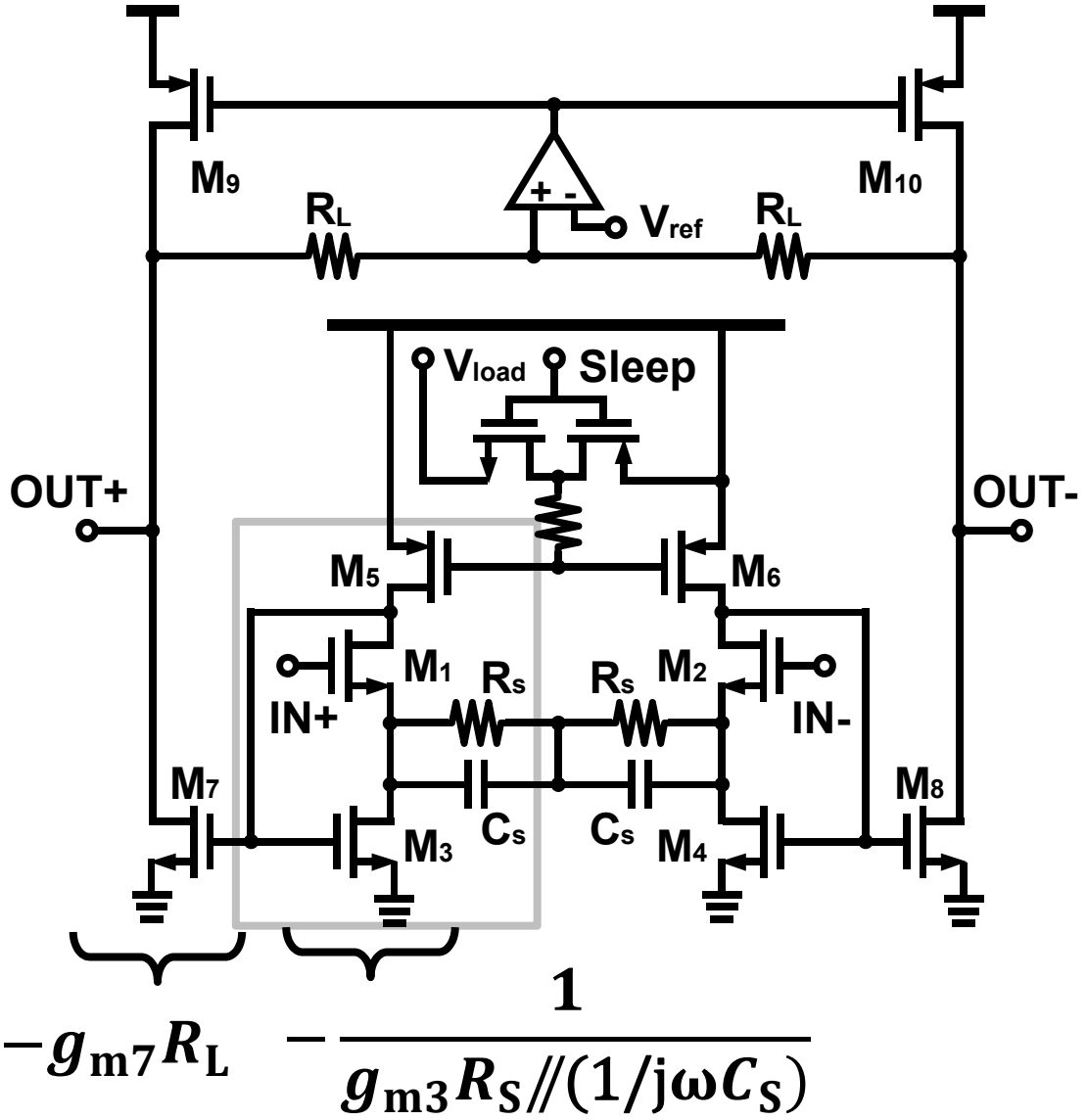


$$A_V \cong -\frac{1}{g_{m3}R_S}$$

modified FVF

$$A_V \cong \frac{g_{m7}}{g_{m3}}\frac{R_L}{R_S}$$

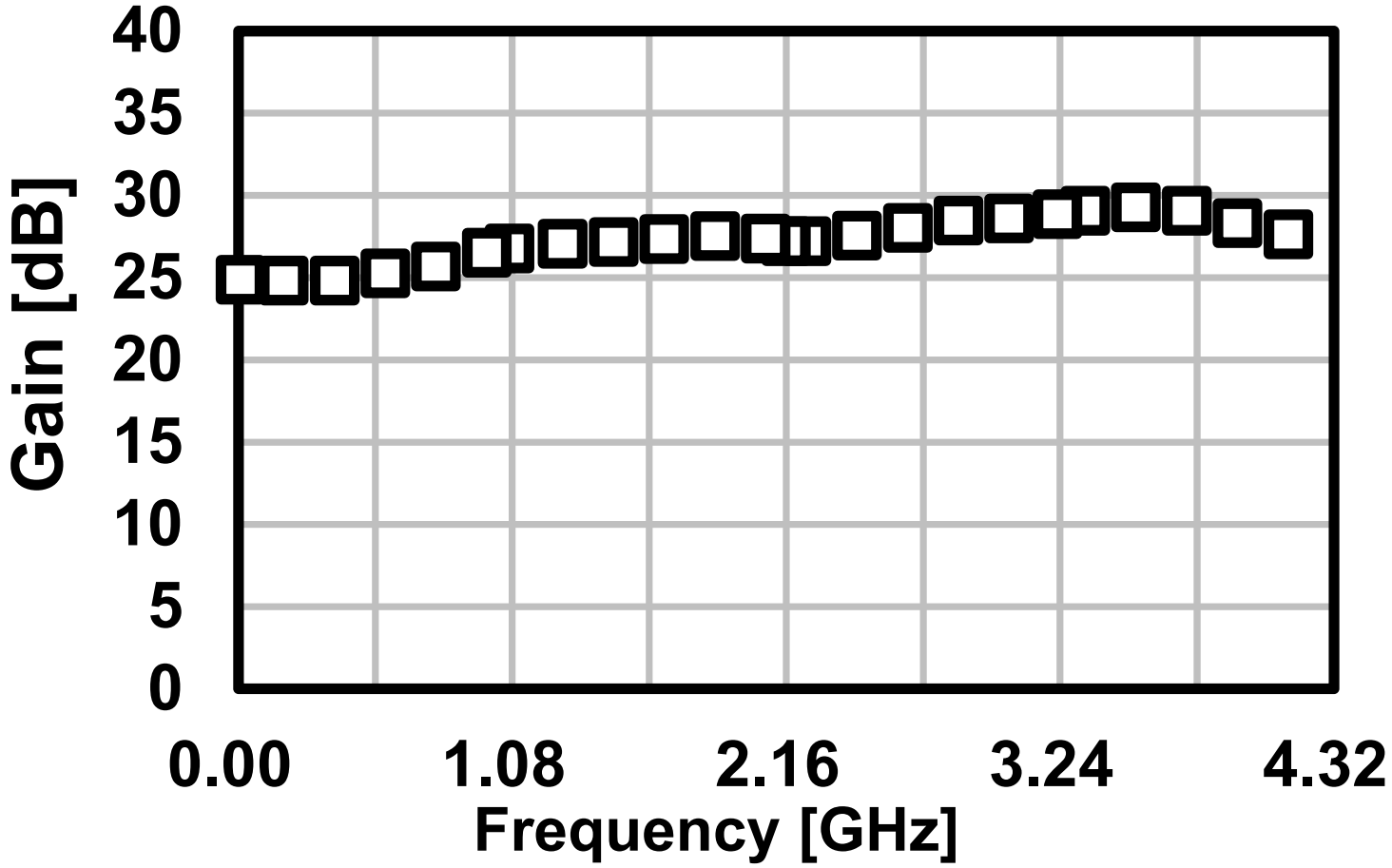
by 6mW



RX Measurement Result

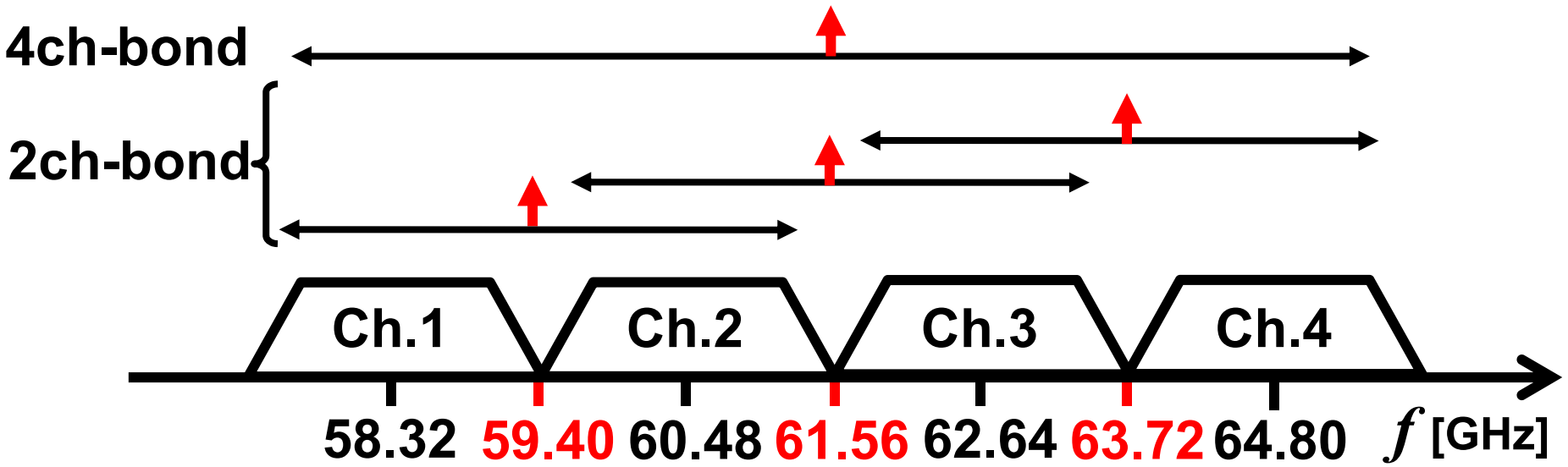
Lower-side-band gain including RF path

LO=61.56GHz



60GHz LO Considerations

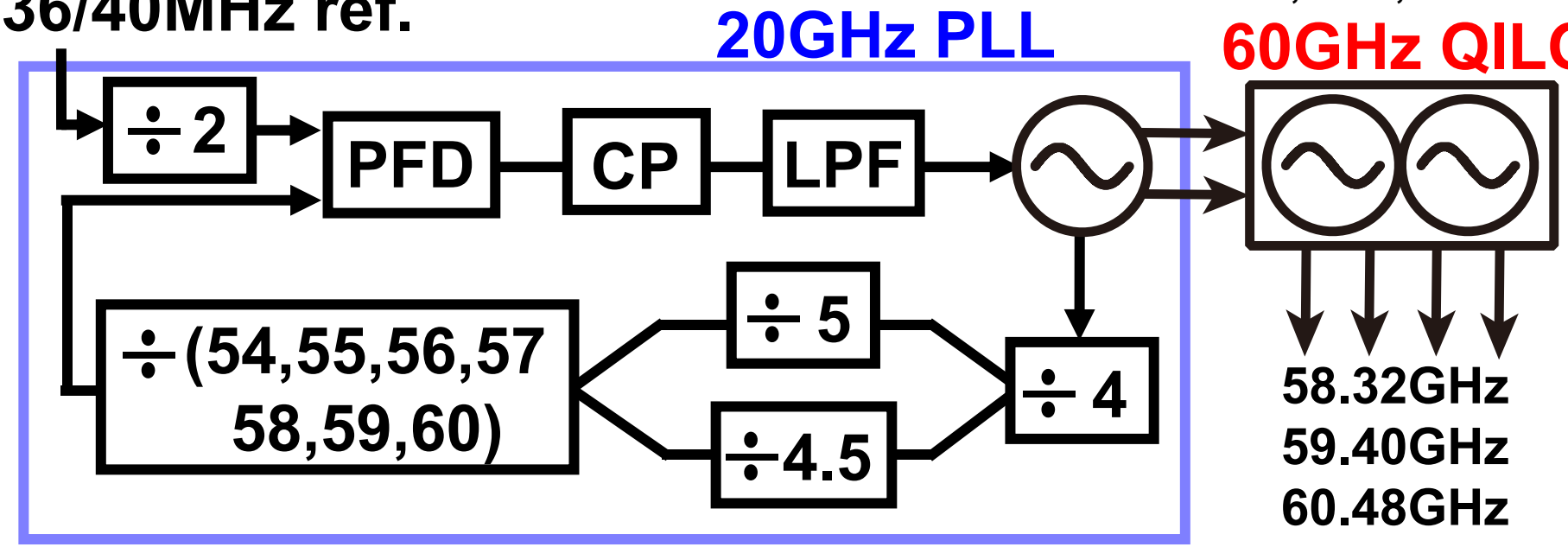
- -96dBc/Hz@1MHz for 64QAM
  - ➔ 60GHz Quadrature Injection Locked Oscillator*
- Channel bonding
  - ➔ 7 carrier frequencies



*K. Okada, *et al.*, JSSC 2013

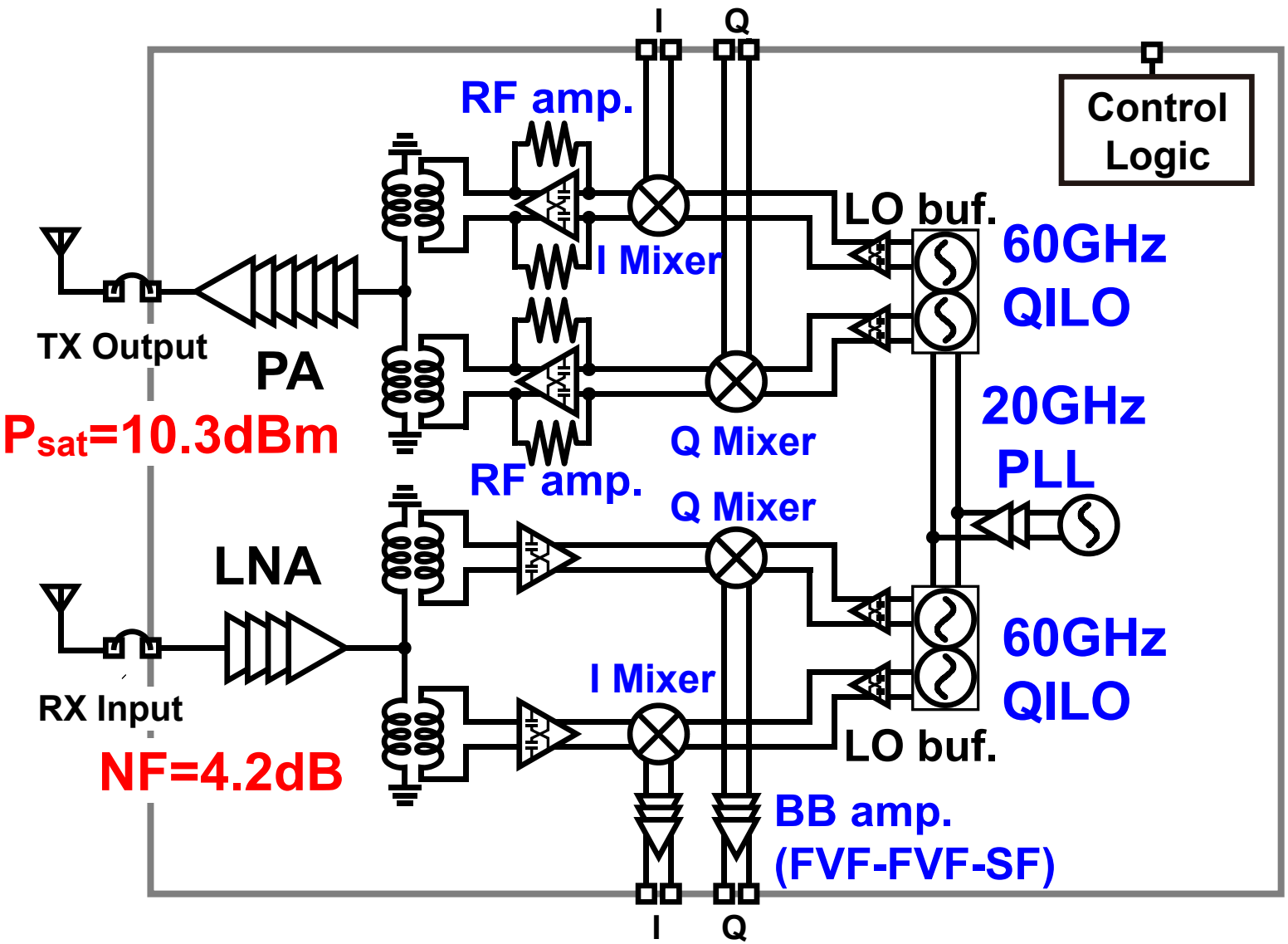
60GHz Quadrature LO Design

*K. Okada, *et al.*, ISSCC 2011

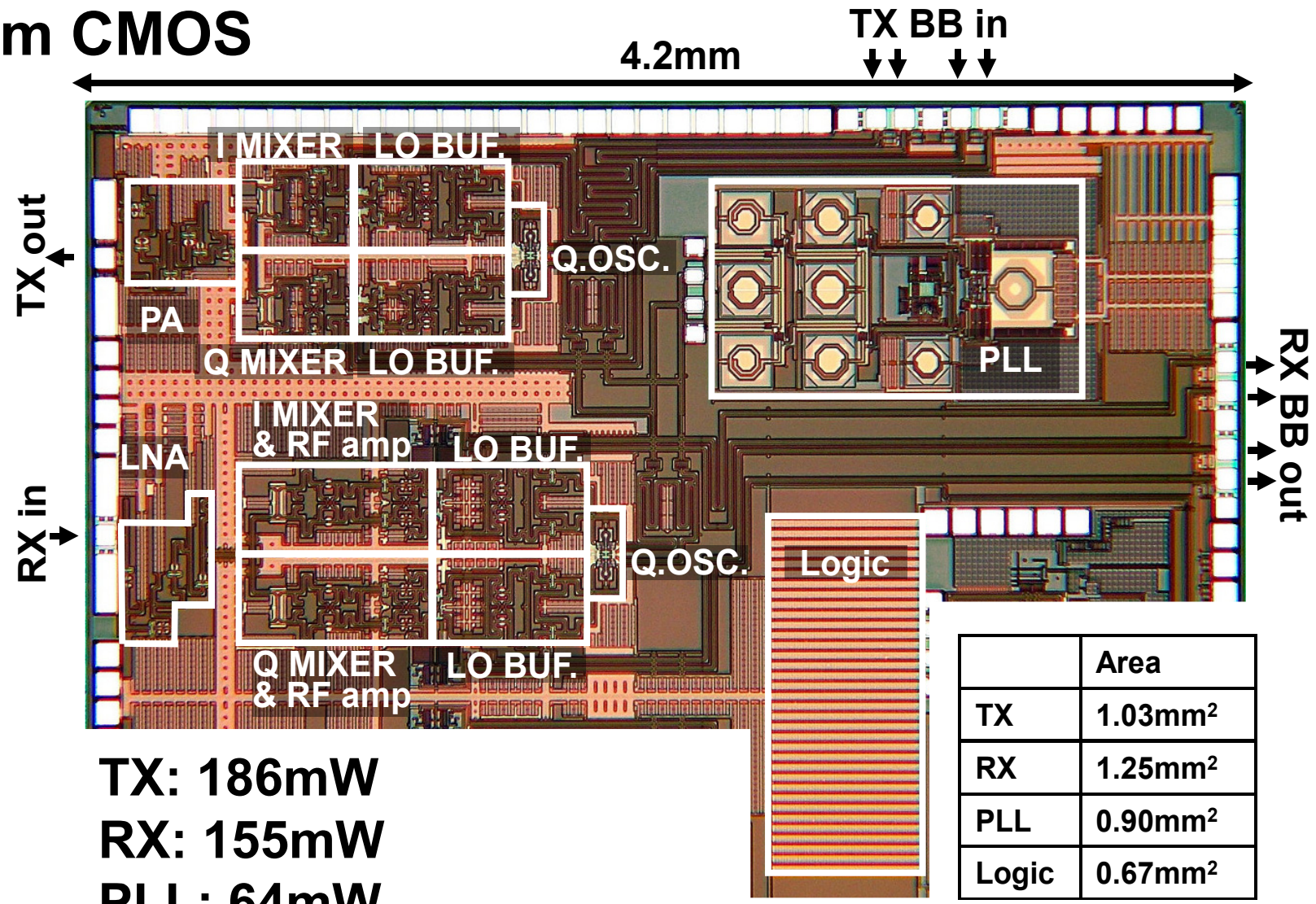


- 20GHz PLL: 64mW
- 60GHz QILO: 18mW(TX)&15mW(RX)
- QILO frequency range: 58-66GHz
- Phase noise improvement by injection locking*
- -96.5dBc/Hz @ 1MHz at 61.56GHz

Detailed Block Diagram



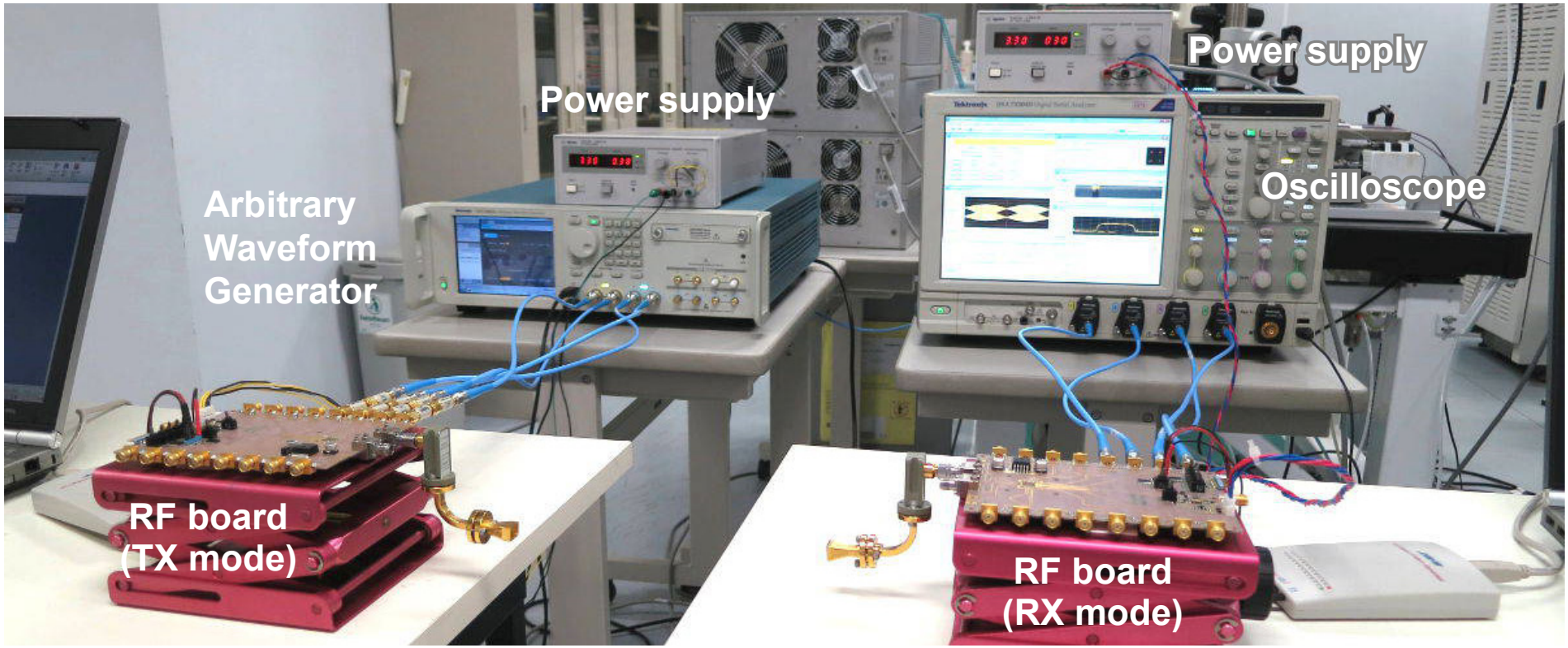
Die Photo



	Area
TX	1.03mm^2
RX	1.25mm^2
PLL	0.90mm^2
Logic	0.67mm^2

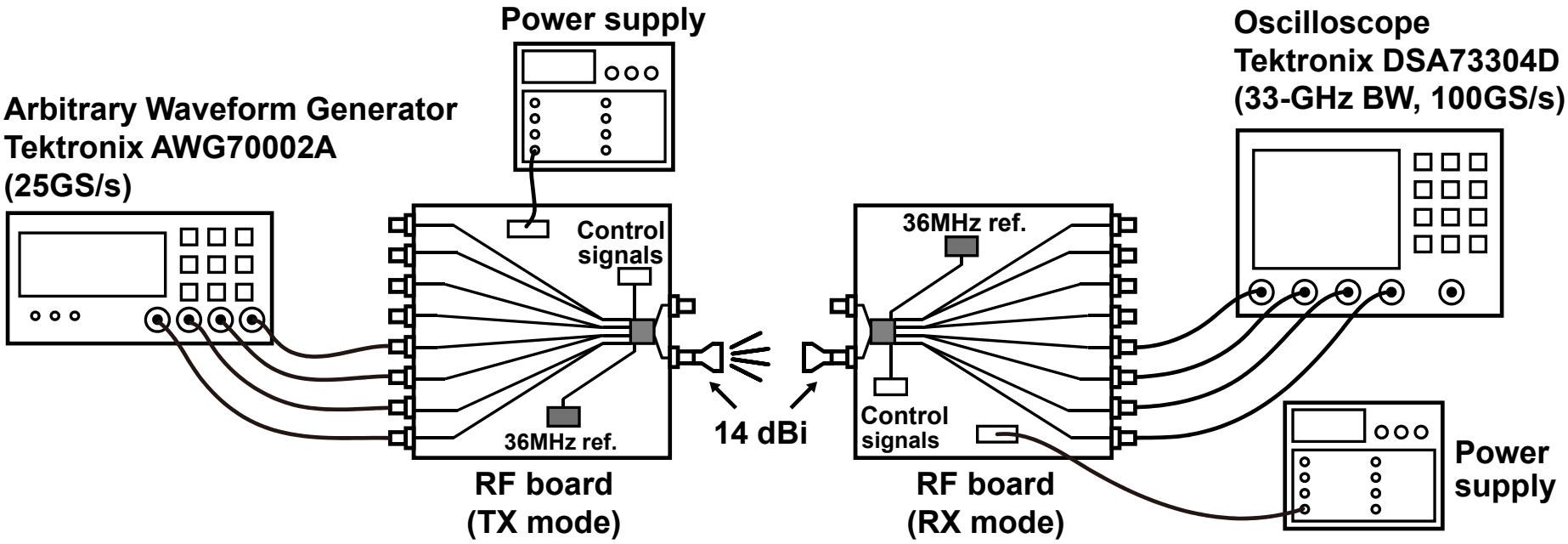
TX: 186mW
RX: 155mW
PLL: 64mW

Measurement Setup



- 25-GS/s AWG
- 100-GS/s oscilloscope (33GHz BW)
- 14-dBi horn antennas

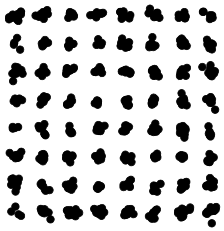
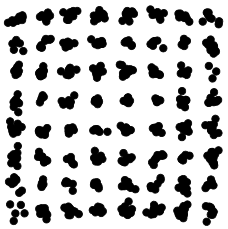
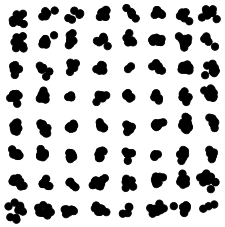
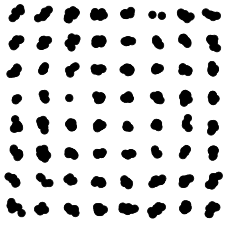
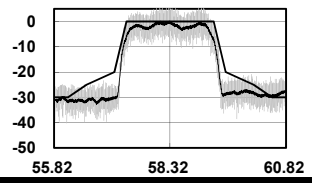
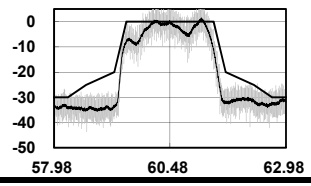
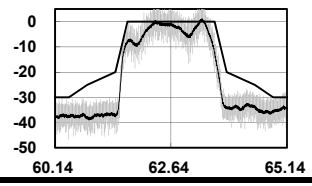
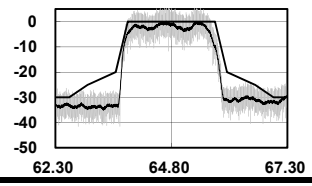
Setup for TX-to-RX Measurement



- Symbol rate: 1.76GS/s (1ch), 7.04GS/s (4ch bonding)
- Roll-off factor: 25% for WiGig spectrum mask
- A maximum distance is defined within a SNR of 9.8dB(QPSK), 16.5dB(16QAM), and 22.5dB(64QAM) for a theoretical BER of 10^{-3}.

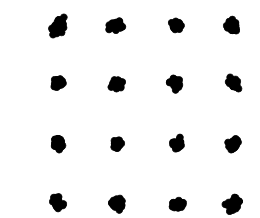
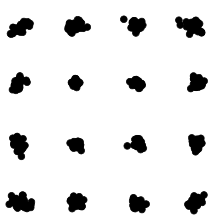
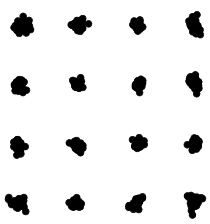
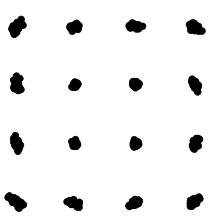
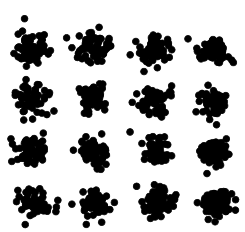
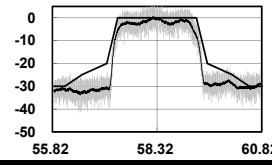
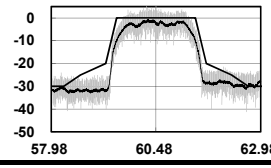
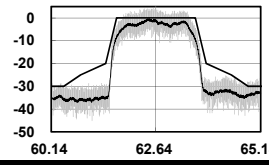
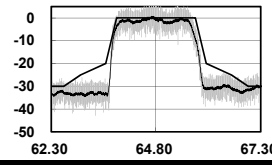
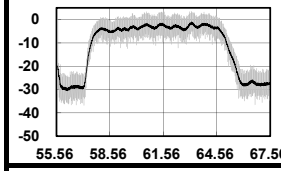
10.56Gb/s 64QAM

64QAM with 10.56Gb/s is achieved for the full 4 channels.

Channel/ Carrier freq.	ch.1 58.32GHz	ch.2 60.48GHz	ch.3 62.64GHz	ch.4 64.80GHz
Modulation	64QAM			
Data rate	10.56Gb/s	10.56Gb/s	10.56Gb/s	10.56Gb/s
Constellation				
Spectrum				
TX EVM	-27.1dB	-27.5dB	-28.0dB	-28.8dB
TX-to-RX EVM	-24.6dB	-23.9dB	-24.4dB	-26.3dB
Distance	0.08m	0.08m	0.13m	0.06m

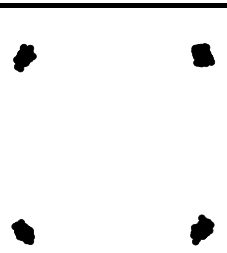
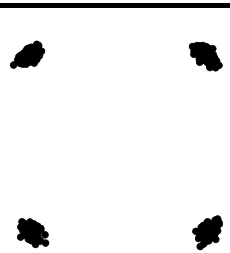
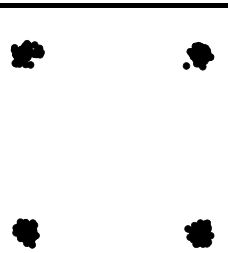
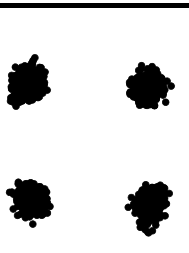
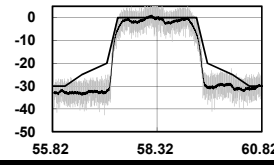
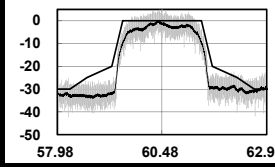
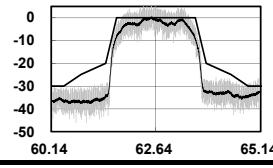
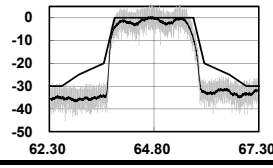
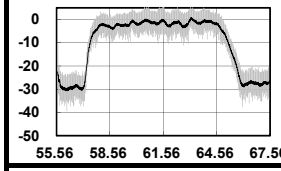
7.04Gb/s 16QAM (max 28.16Gb/s)

28.16Gb/s is achieved by using 4-bonded channel.

Channel/ Carrier freq.	ch.1 58.32GHz	ch.2 60.48GHz	ch.3 62.64GHz	ch.4 64.80GHz	ch.1-ch.4 Channel bond
Modulation	16QAM				
Data rate	7.04Gb/s	7.04Gb/s	7.04Gb/s	7.04Gb/s	28.16Gb/s
Constellation					
Spectrum					
TX EVM	-27.8dB	-27.6dB	-28.4dB	-28.8dB	-20.0dB
TX-to-RX EVM	-24.6dB	-24.1dB	-24.6dB	-27.0dB	-17.2dB
Distance	0.7m	0.6m	0.8m	0.4m	0.07m

3.52Gb/s QPSK (max 14.08Gb/s)

14.08Gb/s is achieved by using 4-bonded channel.

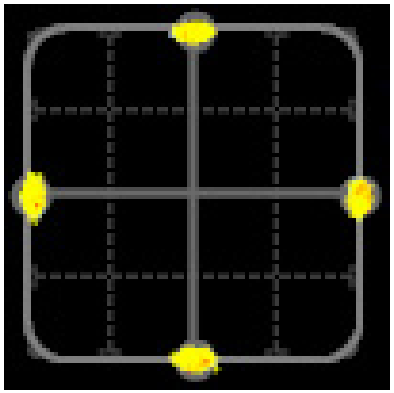
Channel/ Carrier freq.	ch.1 58.32GHz	ch.2 60.48GHz	ch.3 62.64GHz	ch.4 64.80GHz	ch.1-ch.4 Channel bond
Modulation	QPSK				
Data rate	3.52Gb/s	3.52Gb/s	3.52Gb/s	3.52Gb/s	14.08Gb/s
Constellation					
Spectrum					
TX EVM	-28.1dB	-27.7dB	-29.0dB	-29.7dB	-20.1dB
TX-to-RX EVM	-25.3dB	-24.5 dB	-24.5dB	-26.6dB	-17.9dB
Distance	2.4m	2.0m	2.6m	0.9m	0.3m

Performance Comparison of 60GHz TRX

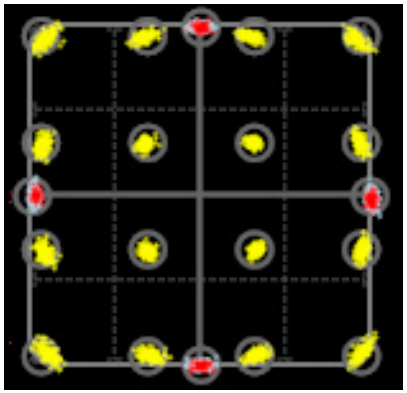
	Data rate / Modulation	TX-to-RX EVM	Power consumption
SiBeam [3]	7.14Gb/s(16QAM)	-19dB	TX: 1,820mW RX: 1,250mW
Tokyo Tech [4, 5]	16Gb/s(16QAM) 20Gb/s(16QAM)[5]	-21dB	TX: 319mW RX: 223mW
IMEC [6]	7Gb/s(16QAM)	-18dB	TX: 167mW RX: 112mW
Panasonic [9]	2.5Gb/s(QPSK)	-22dB	TX: 347mW RX: 274mW
This work	10.56Gb/s(64QAM) 28.16Gb/s(16QAM)	-26dB	TX: 251mW RX: 220mW

Measurement for IEEE802.11ad/WiGig

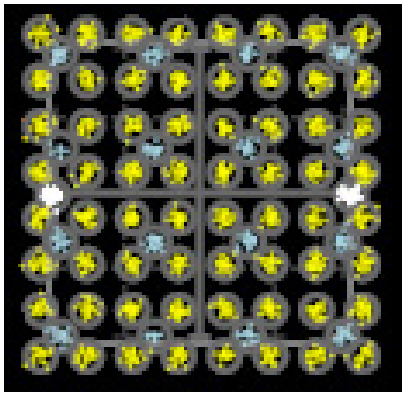
MCS	Modulation		Data rate [Mb/s]	TX EVM [dB]	
				Spec.	Meas.
9	QPSK	SC	2502.5	-15	-27.1
12	16QAM	SC	4620	-21	-27.0
24	64QAM	OFDM	6756.75	-26	-26.5



MCS9



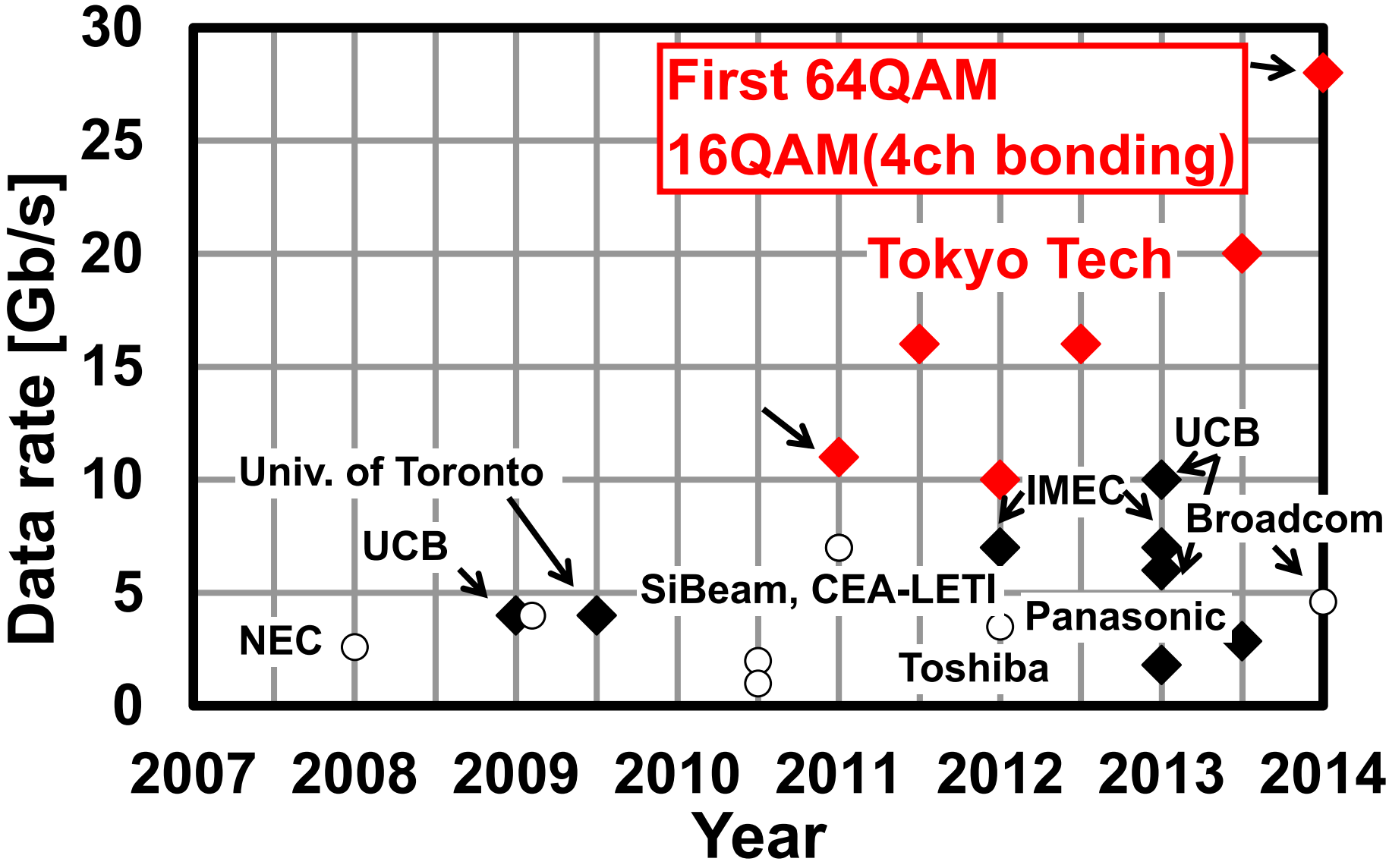
MCS12



MCS24

Measured by Agilent AWG + Osc. + VSA + 81199A in ch.3

60GHz CMOS Transceiver



Conclusion

- A 60GHz direct-conversion transceiver in 65nm CMOS
- The first 64QAM transceiver (10.56Gbps/ch)
  - IEEE802.11ad/WiGig conformance: MCS1-MCS24(64QAM/OFDM)
- The first transceiver capable of 4-channel bonding (28.16Gbps by 16QAM)
  realized by
  - Mixer-first transmitter
  - Open-loop FVF-based baseband amplifier
  - Quadrature injection-locked oscillator

Acknowledgement

This work was partially supported by MIC, SCOPE, MEXT, STARC, Canon Foundation, and VDEC in collaboration with Cadence Design Systems, Inc., and Agilent Technologies Japan, Ltd. The authors thank Dr. Hirose, Dr. Suzuki, Dr. Sato, and Dr. Kawano of Fujitsu Laboratories, Ltd., and Prof. Ando of Tokyo Institute of Technology for their valuable discussions and technical supports.

References

[1] K. Okada, *et al*., "A 60GHz 16QAM/8PSK/QPSK/BPSK Direct-Conversion Transceiver for IEEE 802.15.3c," *IEEE ISSCC*, pp. 160-161, Feb. 2011.

[2] A. Siligaris, *et a*l., "A 65nm CMOS Fully Integrated Transceiver Module for 60GHz Wireless HD Applications," *IEEE ISSCC*, pp.162-163, Feb. 2011.

[3] S. Emami, *et al*., "A 60GHz CMOS Phased-Array Transceiver Pair for Multi-Gb/s Wireless Communications," *IEEE ISSCC*, pp.164-165, Feb. 2011.

[4] K. Okada, *et al*., "A Full 4-Channel 6.3Gb/s 60GHz Direct-Conversion Transceiver with Low-Power Analog and Digital Baseband Circuitry," *IEEE ISSCC*, pp. 218-219, Feb. 2012.

[5] S. Kawai, *et al*., "A Digitally-Calibrated 20Gb/s 60GHz Direct-Conversion Transceiver in 65-nm CMOS," *IEEE RFIC Symp*., pp.137-140, June 2013.

[6] V. Vidojkovic, *et al*., "A Low-Power 57-to-66GHz Transceiver in 40nm LP CMOS with -17dB EVM at 7Gb/s," *IEEE ISSCC*, pp. 268-269, Feb. 2012.

[7] T. Mitomo, *et al*., "A 2Gb/s-Throughput CMOS Transceiver Chipset with In-Package Antenna for 60GHz Short-Range Wireless Communication," *IEEE ISSCC*, pp. 266-267, Feb. 2012.

[8] V. Vidojkovic, *et al*., " A Low-Power Radio Chipset in 40nm LP CMOS with Beamforming for 60GHz High-Data-Rate Wireless Communication," *IEEE ISSCC*, pp. 236-237, Feb. 2013.

References

[9] T. Tsukizawa, *et al*., "A Fully Integrated 60GHz CMOS Transceiver Chipset Based on WiGig/IEEE802.11ad with Built-in Self-Calibration for Mobile Applications," *IEEE ISSCC*, pp. 230-231, Feb. 2013.

[10] M. Soer, *et al*., "A 0.2-to-2.0GHz 65nm CMOS Receiver Without LNA Achieving >11dBm IIP3 and <6.5dB NF," *IEEE ISSCC*, pp.222-223, Feb. 2009.

[11] C. Andrews, and A.C. Molnar, "A Passive-Mixer-First Receiver with Baseband-Controlled RF Impedance Matching, < 6dB NF, and > 27dBm Wideband IIP3," *IEEE ISSCC*, pp. 46-47, Feb 2010.

[12] R. Carvajal, *et al*., "The Flipped Voltage Follower: A Useful Cell for Low-Voltage Low-Power Circuit Design," *IEEE Trans. CAS-I*, Vol. 52, No. 7, pp. 1276-1291, July 2005.

[13] K. Okada, *et al*., "Full Four-Channel 6.3-Gb/s 60-GHz CMOS Transceiver with Low-Power Analog and Digital Baseband Circuitry," *IEEE JSSC*, Vol. 48, No. 1, pp.46-65, Jan. 2013.

20.4: A Fully Integrated Single-Chip 60GHz CMOS Transceiver with Scalable Power Consumption for Proximity Wireless Communication

Shigehito Saigusa, Toshiya Mitomo, Hidenori Okuni, Masahiro Hosoya, Akihide Sai, Shusuke Kawai, Tong Wang, Masanori Furuta, Kei Shiraishi, Koichiro Ban, Seiichiro Horikawa, Tomoya Tandai, Ryoko Matsuo, Takeshi Tomizawa, Hiroaki Hoshino, Junya Matsuno, Yukako Tsutsumi, Ryoichi Tachibana, Osamu Watanabe, Tetsuro Itakura

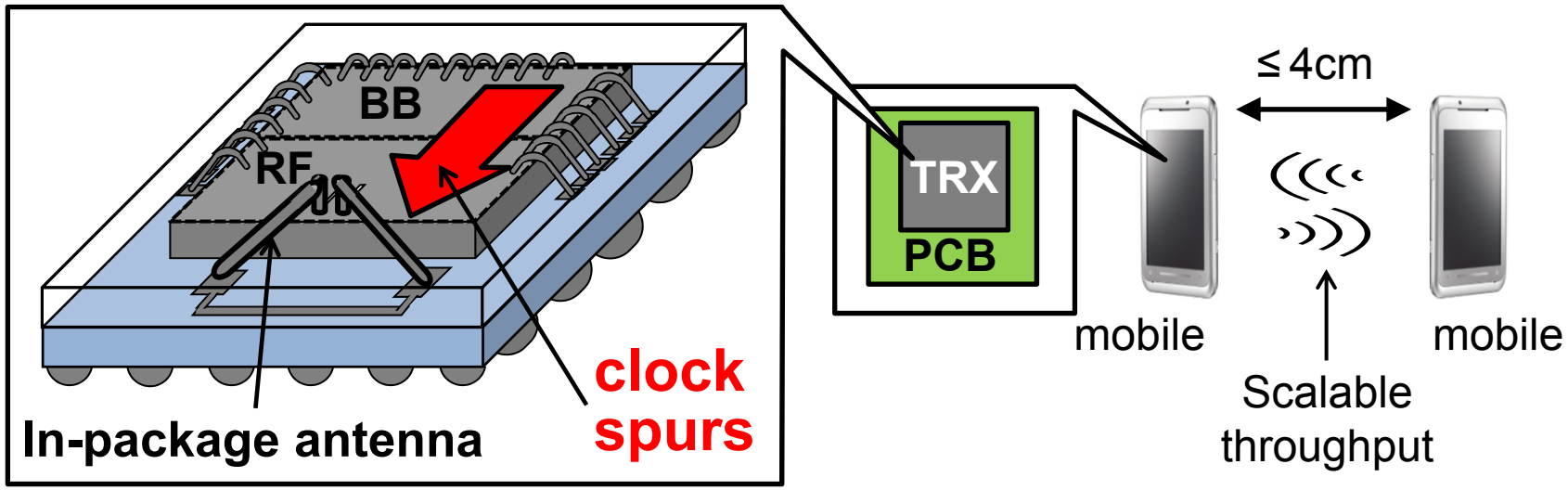
Toshiba Corporation, Kawasaki, Japan

Outline

- **Motivations & Challenges**
- **Single-chip implementation techniques**
  - Reducing number and level of clock spurs
    - Spurs-less frequency planning of clock spurs
    - Low power PHY designing
  - Spurs tolerant low noise RF blocks
- **Measured Results**
  - In-band clock-spurs level
  - Scalably-reduced power consumption with MAC throughput
- **Conclusions**

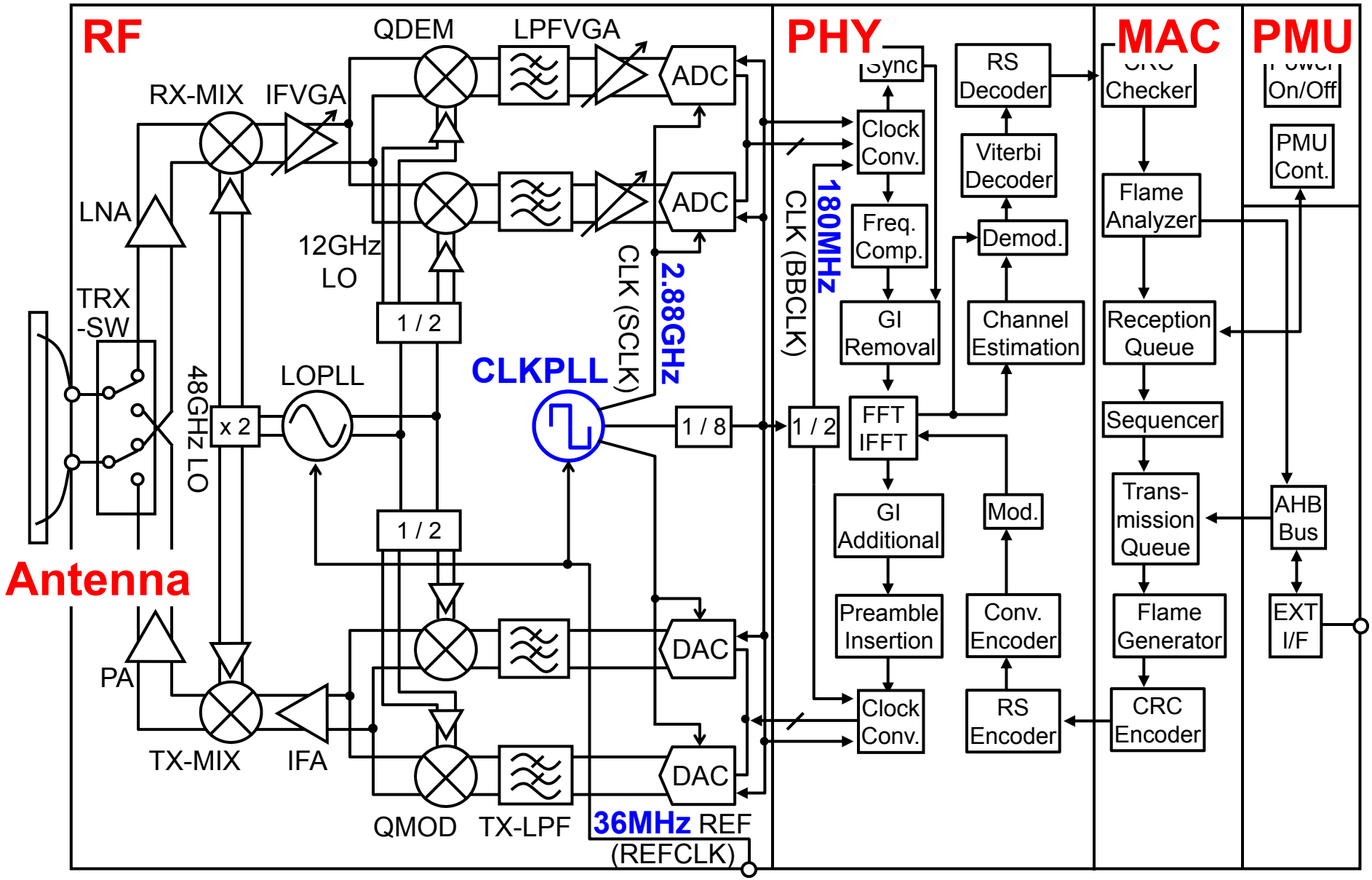
Motivations & Challenges

- A single-chip 60GHz CMOS transceiver (TRX) for peer-to-peer proximity communication system
  - **High data rate, small size and easy mountability**

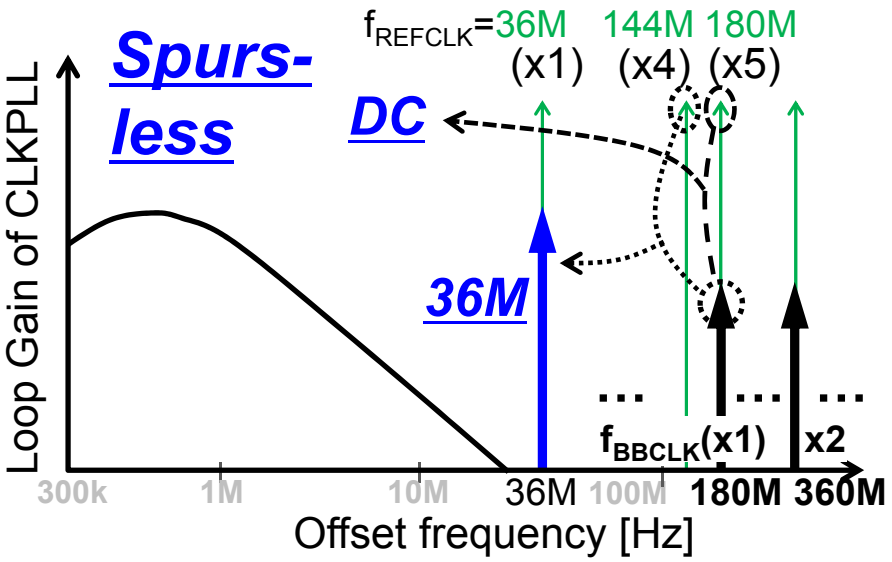


- Challenges for implementing a single-chip TRX
  - **To minimize SNR degradation** due to clock spurs
  - **To reduce power consumption scalably** with MAC throughput

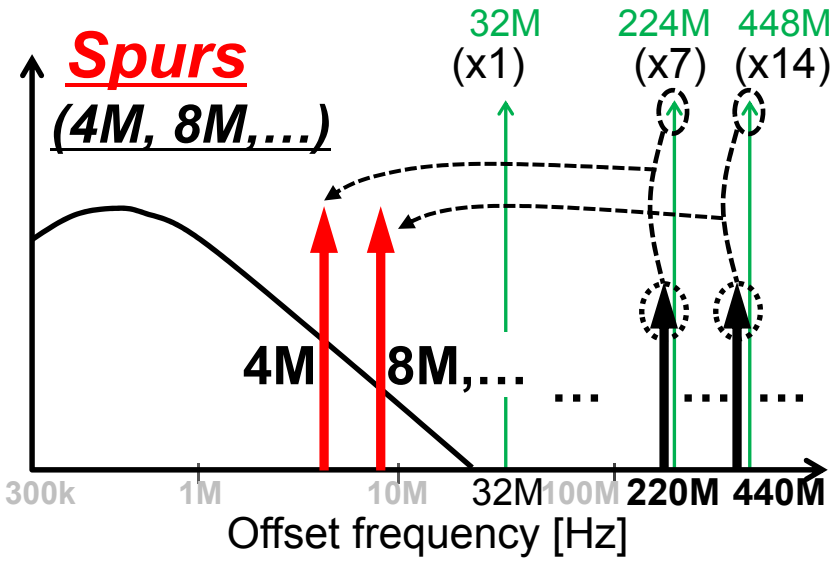
Block diagram of the single-chip TRX



Spurs-less frequency planning of 3 CLKs



This work



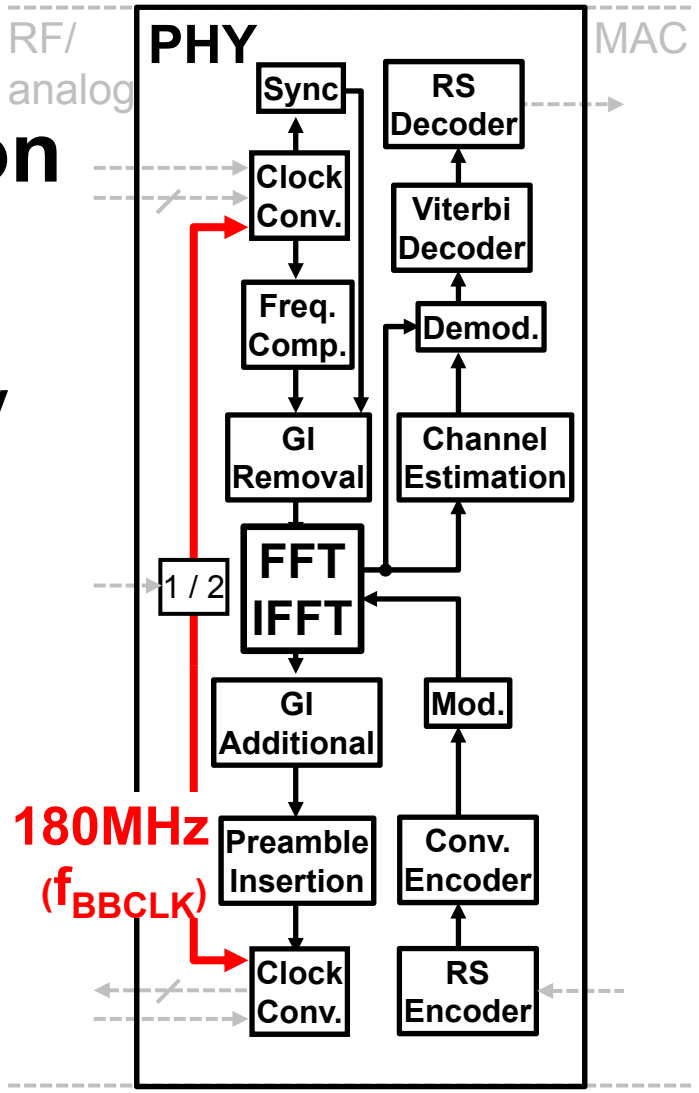
Other work

	f_{SCLK}	f_{BBCLK}	f_{REFCLK}	f_{BBCLK}/f_{REFCLK}
This work	2.88GHz	180MHz	36MHz	**5 (integer)**
Other work	3.52GHz	220MHz	32MHz	**6.875 (not integer)**

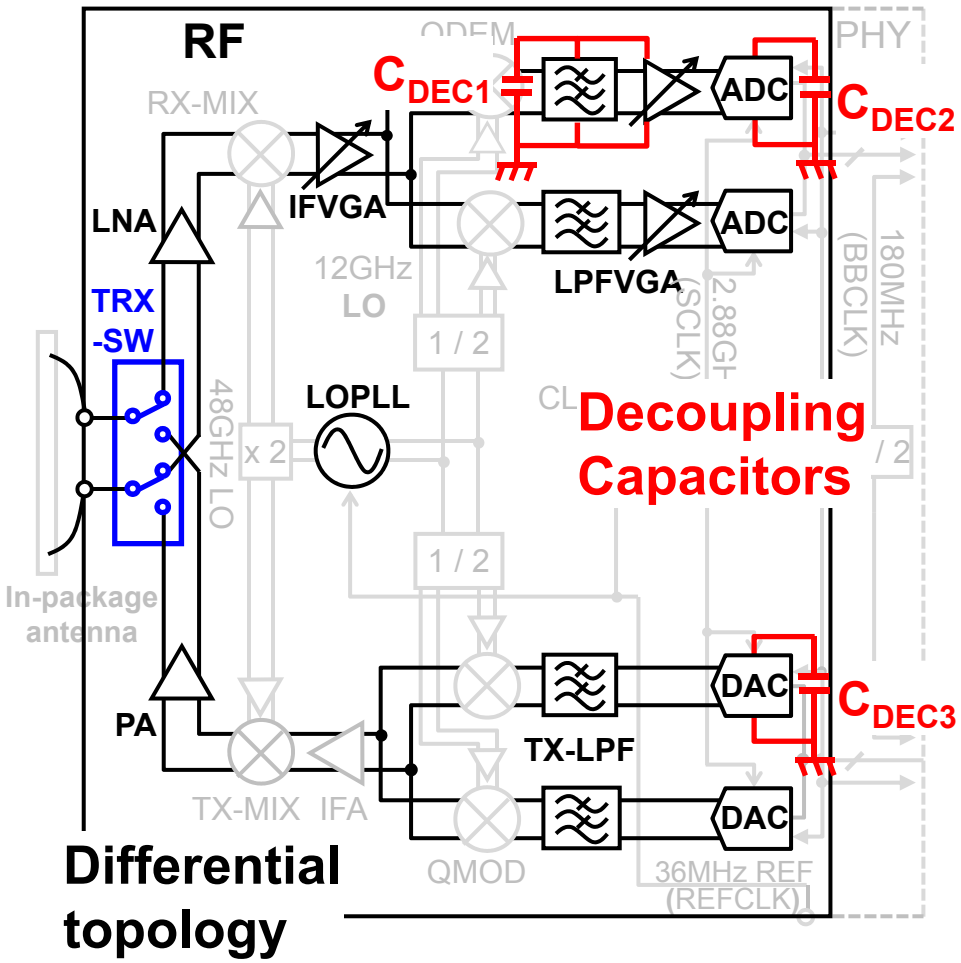
- Spurs with frequency of more than f_{REFCLK}
  - CLKPLL with low jitter performance
    - **Better SNR performance**

Low power PHY designing

- Optimization with **size** and **power consumption**
  - f_{BBCLK} of **180MHz** as a lowest possible frequency
  - **Low power 64-point FFT/IFFT**
  - **Clock gating** for entire blocks



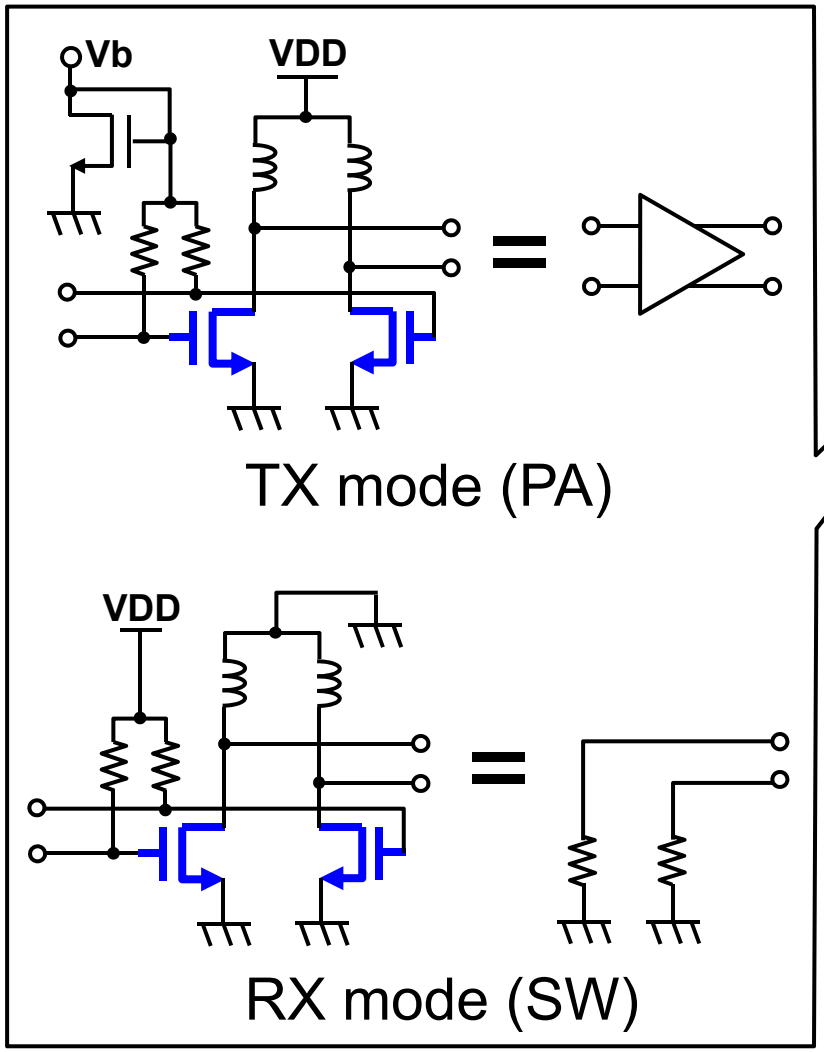
Spurs tolerant low noise RF blocks



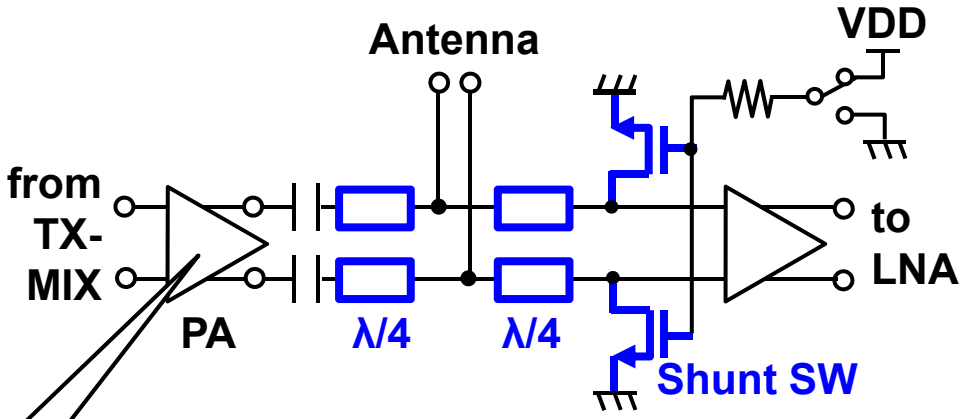
Block	[3]	This work
TRX -SW	SW & Transformer	**SW & λ/4 Transmission Line**
LNA /PA	Current Reuse	Common Source ([4])
ADC	Flash	Time-Interleaved SAR
LOPLL	20GHz QVCO	24GHz VCO
RX-IFA	-	IF-VGA (1bit)
TX-LPF	-	Passive LC

[3] T. Mitomo, et al., ISSCC, 2012
[4] S. Kawai, et al., A-SSCC, 2013

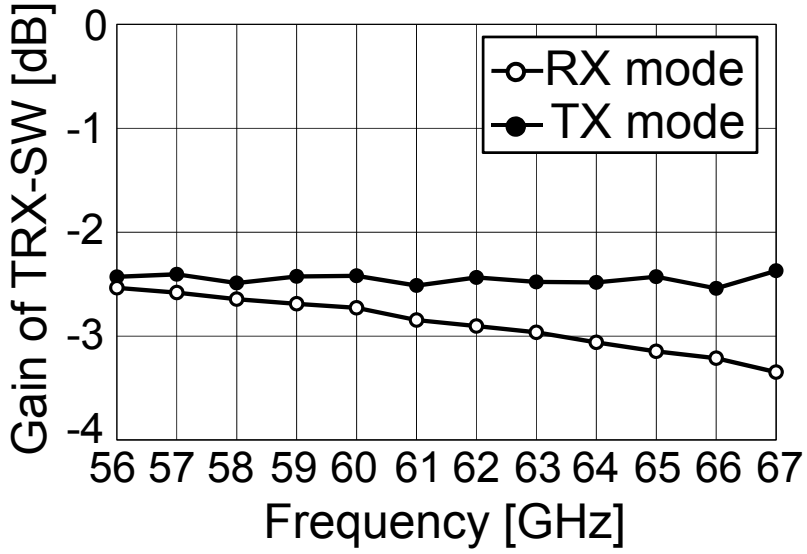
Low-loss TRX-SW circuit



PA circuit

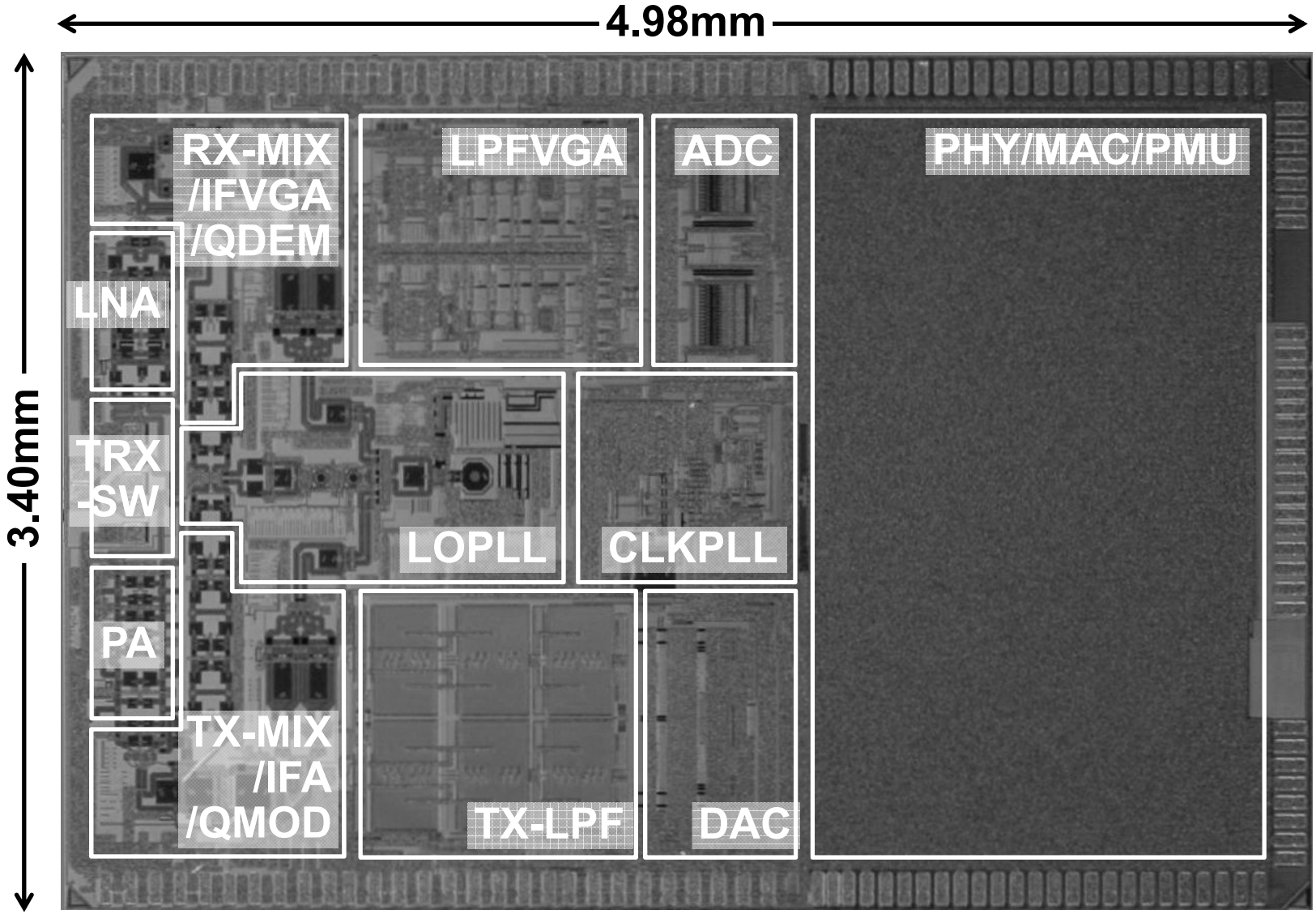


TRX-SW circuit



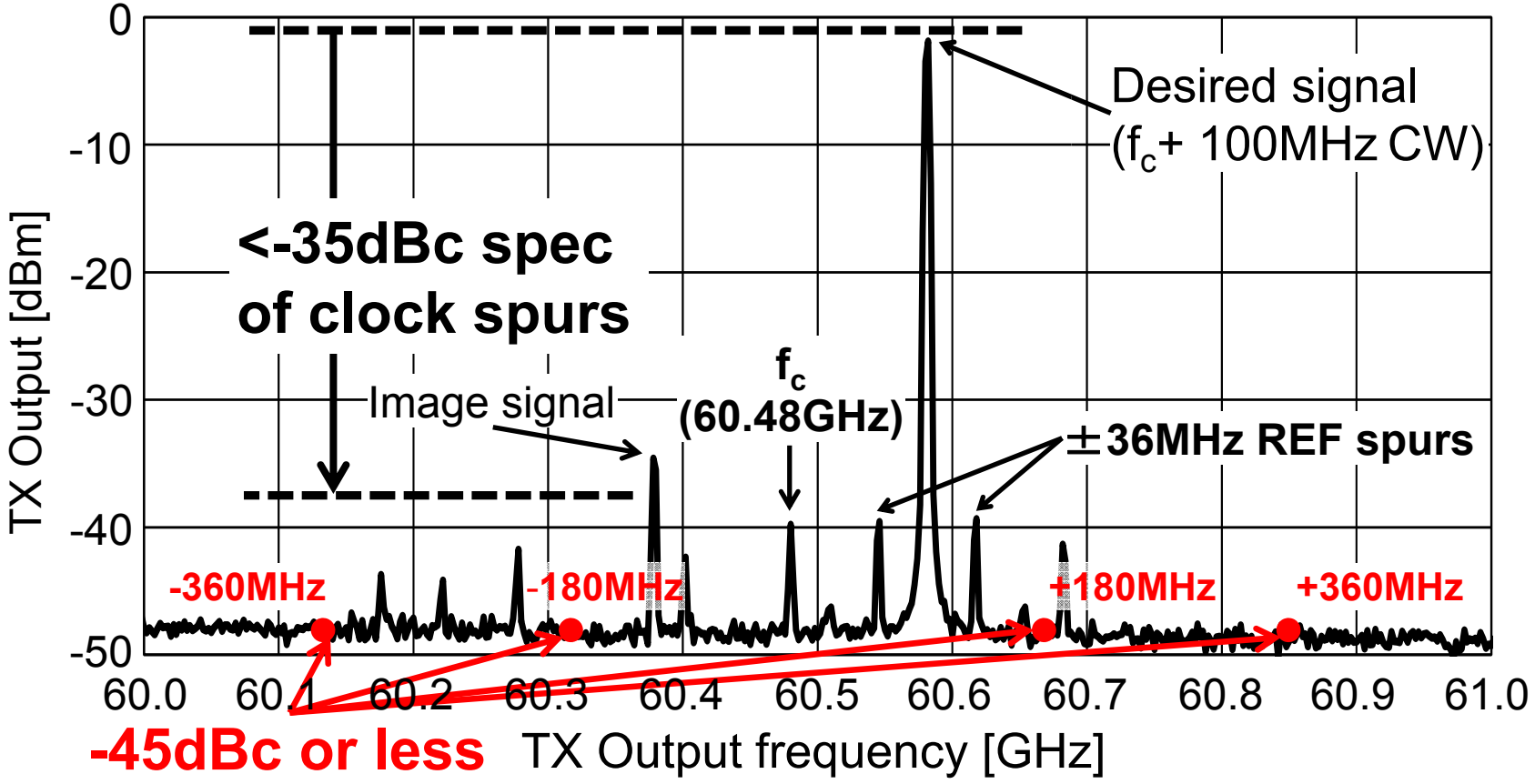
Measured Insertion losses

Die micrograph



1P6M 65nm Standard CMOS

Measured in-band clock spurs level of TX

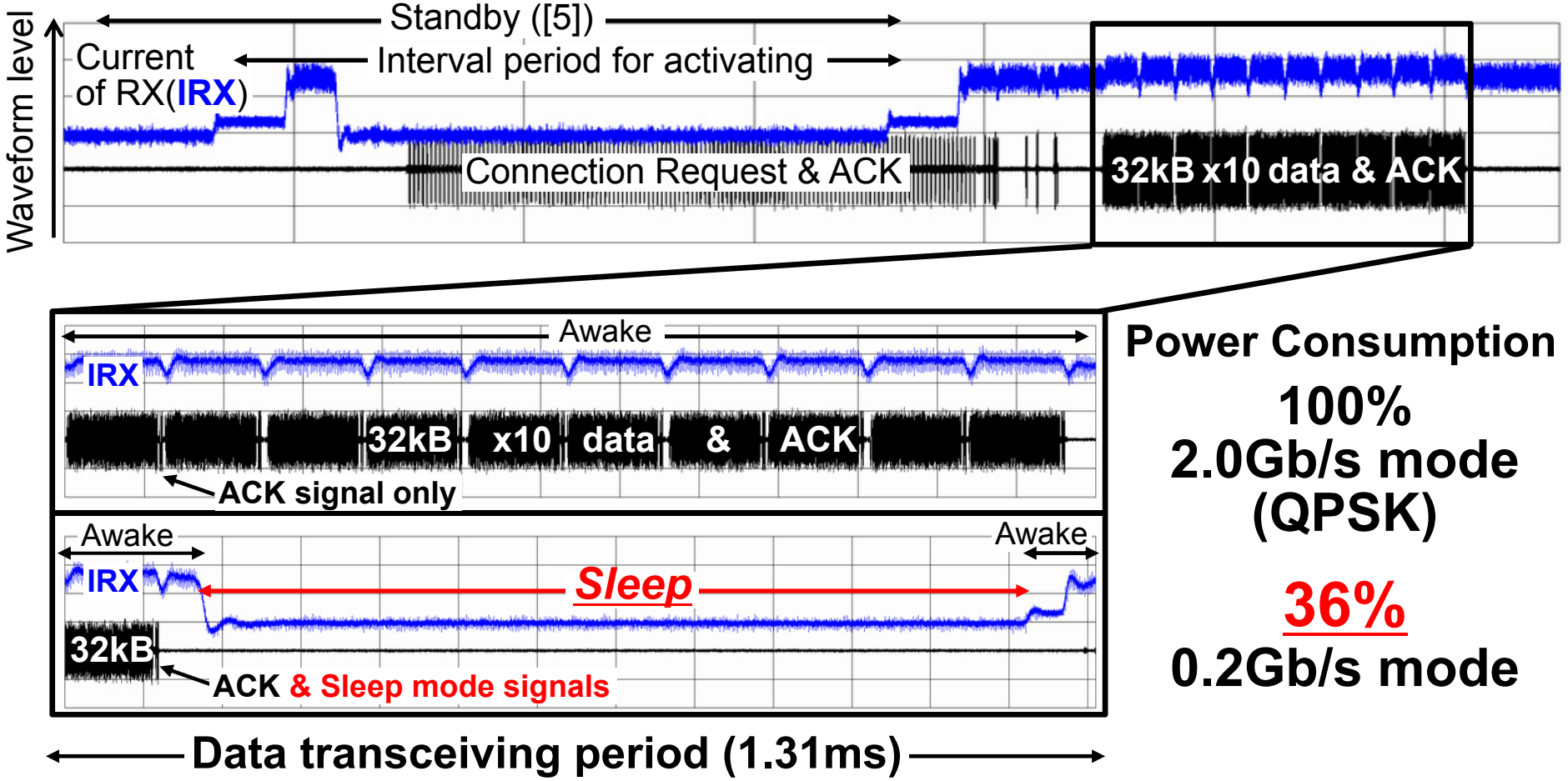


In-band spurs level of TX output signal at CH2

- Frequency difference : 36MHz or larger
- Clock spurs level : **-45dBc or less**

Scalably-reduced power consumption

- **Sleep-mode signals into ACK Header**
- **Sleep mode control in minimum period of 10μs**



Power Consumption

100%
2.0Gb/s mode
(QPSK)

36%
0.2Gb/s mode

[5] R. Matsuo, et al., ICC, 2012

Performance summary

Technology	65nm CMOS
Supply voltage	1.2V / 1.8V / 3.3V
Chip size	4.98mm x 3.40mm

Rx performance at CH2	
Voltage gain	40 dB
DSB NF	**8.9dB**
(including **2.8dB** of TRX-SW's loss)	
Image rejection ratio	30.3 dB
-	
3-dB bandwidth	2.2 GHz
Power consumption	687 mW
(RF)	(468 mW)
(ADC & CLKPLL)	(94 mW)
(PHY & MAC & PMU)	(**125mW**)

Tx performance at CH2	
Power gain(estimated)	16.3 dB
P1dB output	2.8 dBm
Saturation output	4.9 dBm
Image rejection ratio	30.5 dB
Carrier leakage	-29.8 dBc
3-dB bandwidth	1.9 GHz
Power consumption	581 mW
(RF)	(360 mW)
(DAC & CLKPLL)	(139 mW)
(PHY & MAC & PMU)	(**82mW**)

Performance comparison

	Number of Chip	Chip Integration	Assembly	Distance / Throughput	Power consumption	Scalability of power consumption w/ Sleep mode
[1]	2	RF/ PHY/ MAC	Antenna module	40cm/1.8Gb/s 1m/1.5Gb/s	TX:788mW RX:984mW	N/A
[2]	2	RF/ PHY	BGA w/ waveguide antenna	1.7m/3.1Gb/s[1)] 10cm/6.3Gb/s	TX:515mW[2)] RX:621mW[2)]	N/A
[3]	2	RF/ PHY/ MAC	Standard BGA w/ bonding wire antenna	4cm/2.1Gb/s	TX:592mW RX:756mW	N/A
This work	**1**	RF/ PHY/ MAC/ PMU		4cm/2.0Gb/s (QPSK) (BW 2.16GHz)	TX:581mW RX:687mW	46%(0.4Gb/s) **36%**(0.2Gb/s)

[1] T. Tsukizawa, et al., ISSCC, 2013. [2] K. Okada, et al., ISSCC, 2012.
[3] T. Mitomo, et al., ISSCC, 2012

[1)]PHY data rate
[2)]w/o MAC

Conclusions

- **A first fully integrated (Antenna, RF, PHY, MAC and PMU) single-chip 60GHz CMOS transceiver** with maximum MAC throughput of 2.0Gb/s

- **Frequency difference of 36MHz or larger**
- **Clock spurs of -45dBc or less**
  - Reducing number and level of clock spurs
  - Clock-spurs tolerant low noise RF blocks

- **Scalably-reduced power consumption with MAC throughput** by introducing “Sleep mode”

Acknowledgement

This research is partially supported by the Ministry of Internal Affairs and Communications of Japan.

20.5: A 40nm Dual-Band 3-Stream 802.11a/b/g/n/ac MIMO WLAN SoC with 1.1Gb/s Over-the-Air Throughput

Ming He, Renaldi Winoto, Xiang Gao, Wayne Loeb, David Signoff, Wai Lau, Yuan Lu, Donghong Cui, Kun-Seok Lee, Sai-Wang Tam, Philip Godoy, Yung Chen, Sanghoon Joo, Changhui Hu, Arvind Anumula Paramanandam, Xiaoyue Wang, Chi-Hung Lin, Li Lin

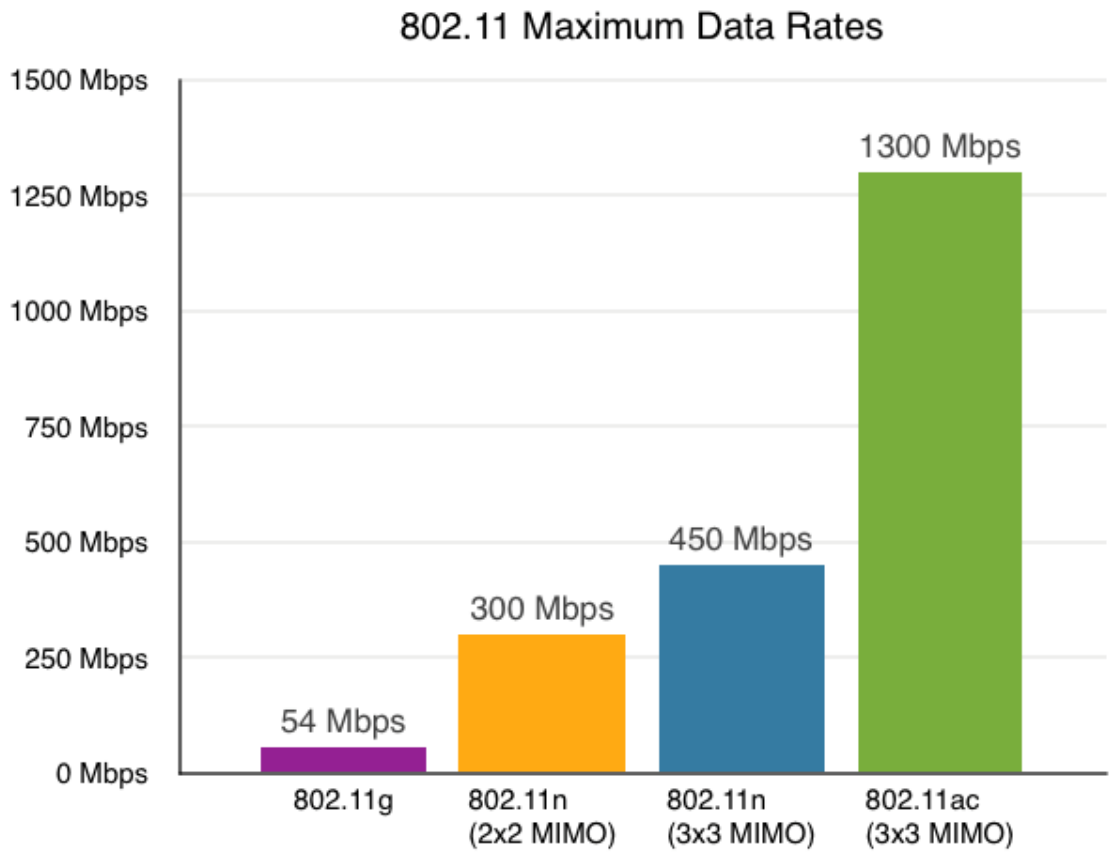
Marvell Semiconductor, Santa Clara, CA

Outline

- Introduction
- RF transceiver design
- Circuit implementation
- Measurement results
- Conclusions

802.11ac MIMO Wireless LAN

■ Why 802.11ac?



RF Design Challenges

11ac Features

- 256 QAM
- 80MHz BW
- 11a/n compatibility

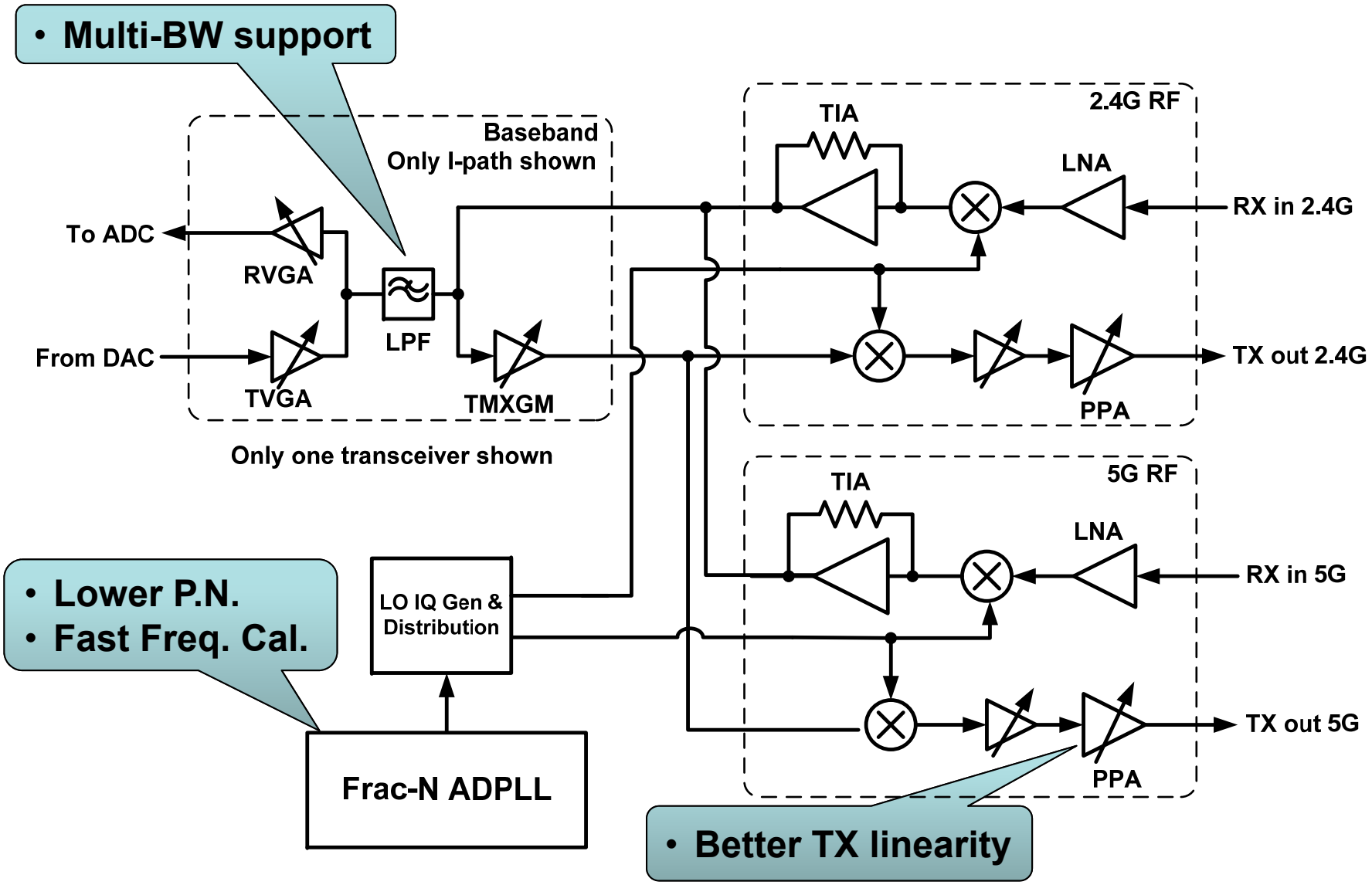
Enterprise Features

- Public Safety support
- Fast Ch. Switching
- Interference Tolerance

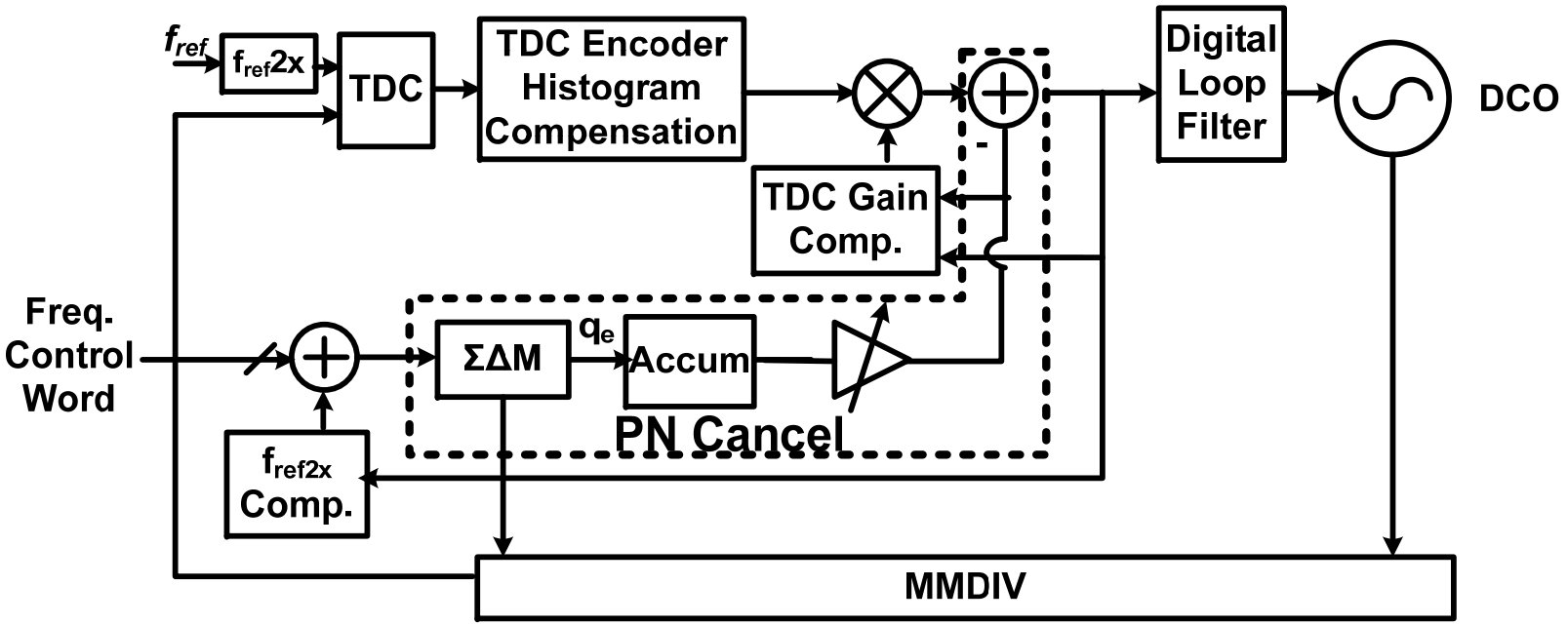
RF XCVR Specs

- Lower Phase Noise
- Better TX linearity
- Multi-BW support
- Fast Freq. Calibration

RF Transceiver Block Diagram

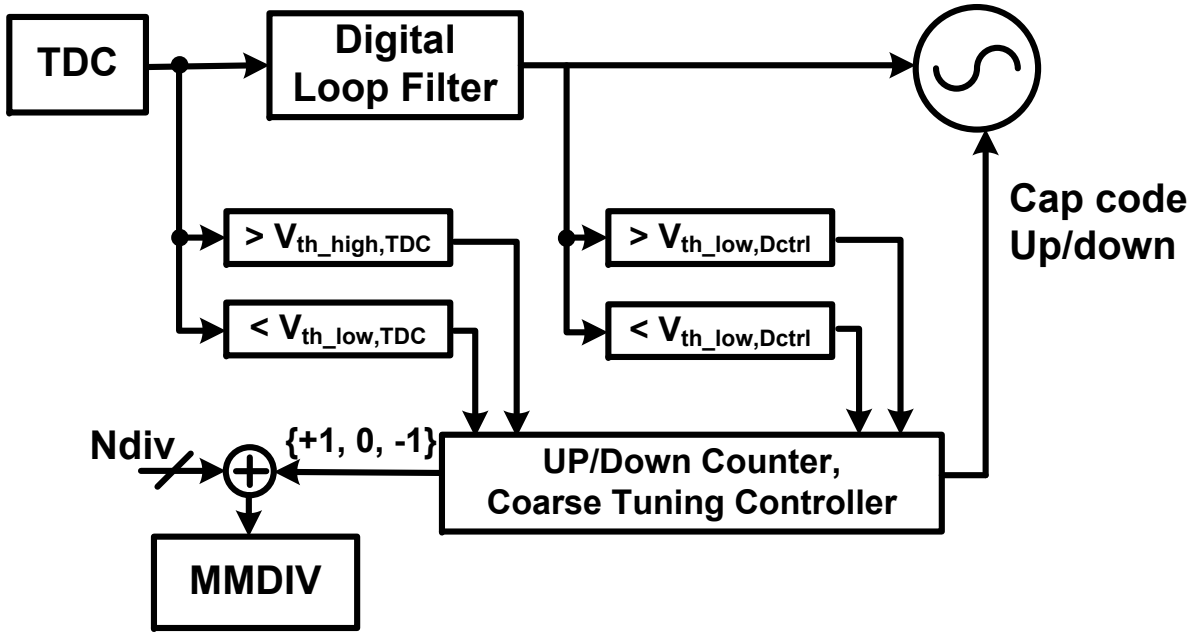


ADPLL Architecture



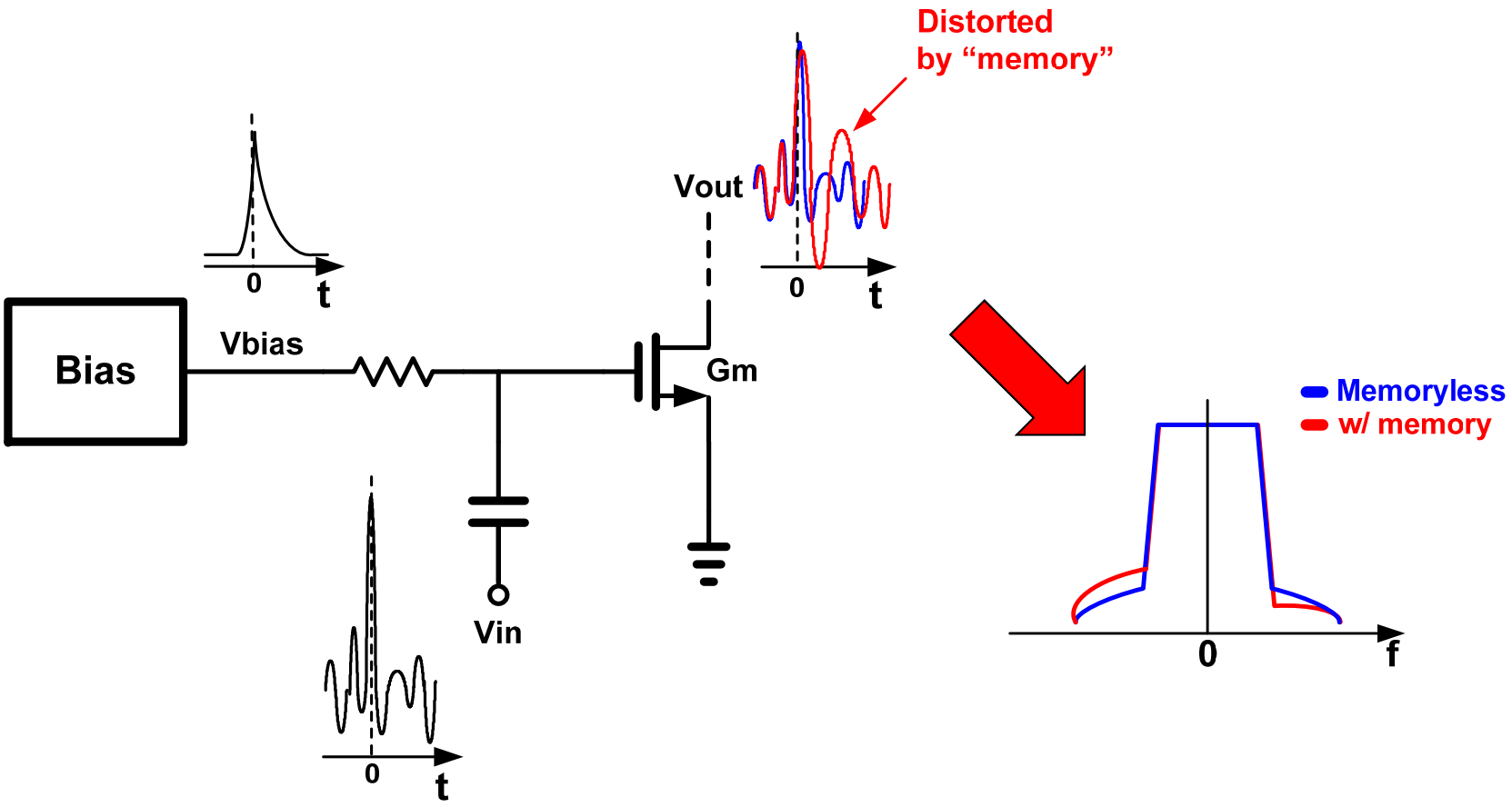
- **Phase noise reduction**
  - Frequency doubler with duty cycle compensation
  - TDC non-linearity histogram compensation
  - TDC gain calibration and quantization PN cancellation
- **Single 10-bit DCO covers both bands**
  Fast FCAL needed to cut channel switching time

ADPLL: DCO Cap Code Search



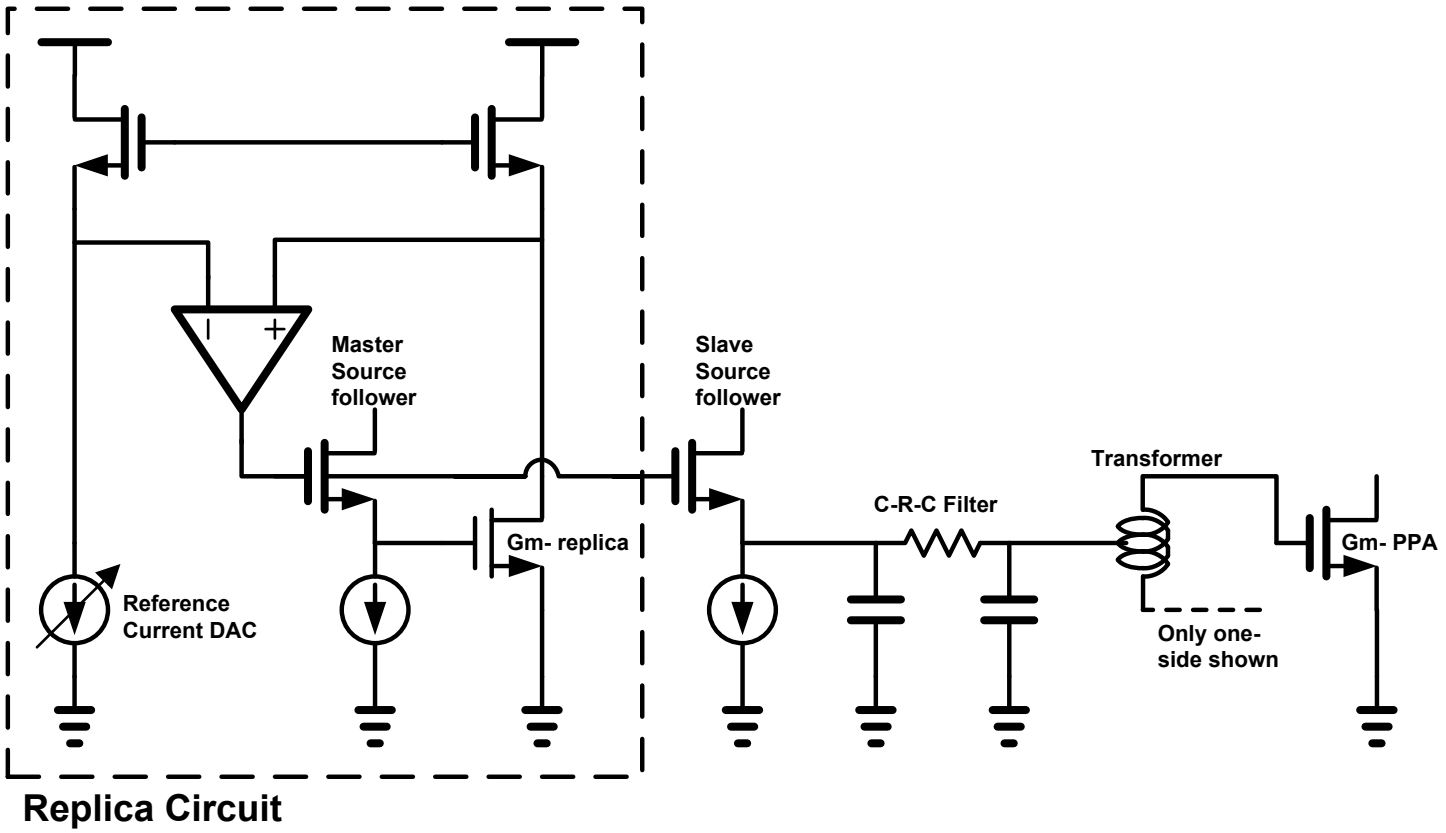
- **TDC bound check added**
  - Temporarily change division ratio to pull in FBCLK phase
  - Speed up phase locking
- **Adaptive wait time for cap code decision**
  - Short wait time at beginning
  - Longer wait time when search direction changed

Transmitter: Memory Effects



- **Memory effects can degrade**
  - **TX EVM**
  - **TX spectrum mask**

Transmitter: Pre-PA Bias Circuit

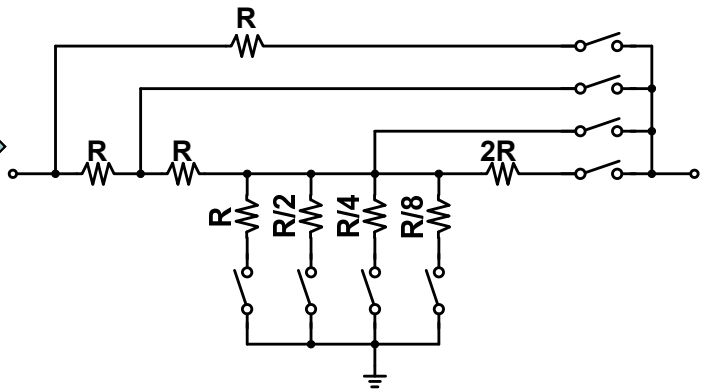


- **Wide-band bias scheme to minimize memory effects**
  - Low impedance at baseband frequency
  - High impedance at RF carrier frequency

Receiver LPF: Bi-quad Input Resistor

BW mode	SNR Requirement
5MHz	Low
10MHz	Low
20MHz	Med
40MHz	High
80MHz	High

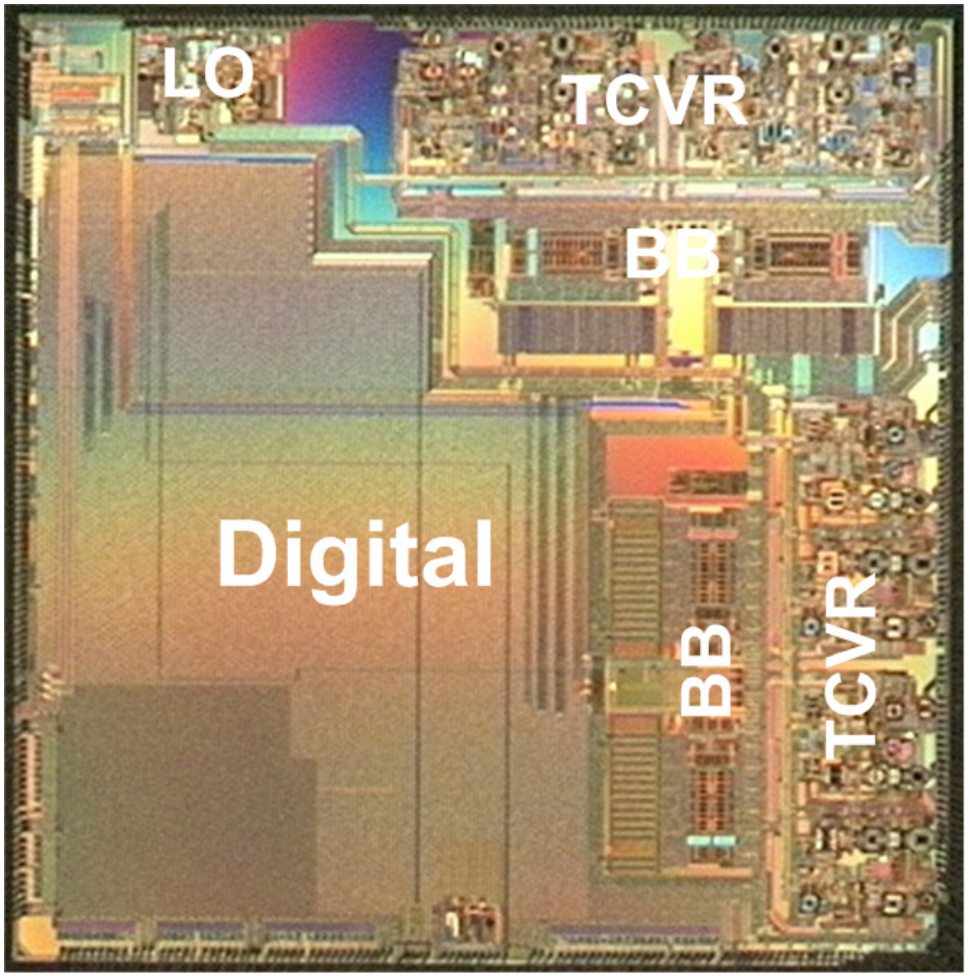
T-network



Implementation	# of Unit R
Conventional	128
T-network	20
Hybrid	23

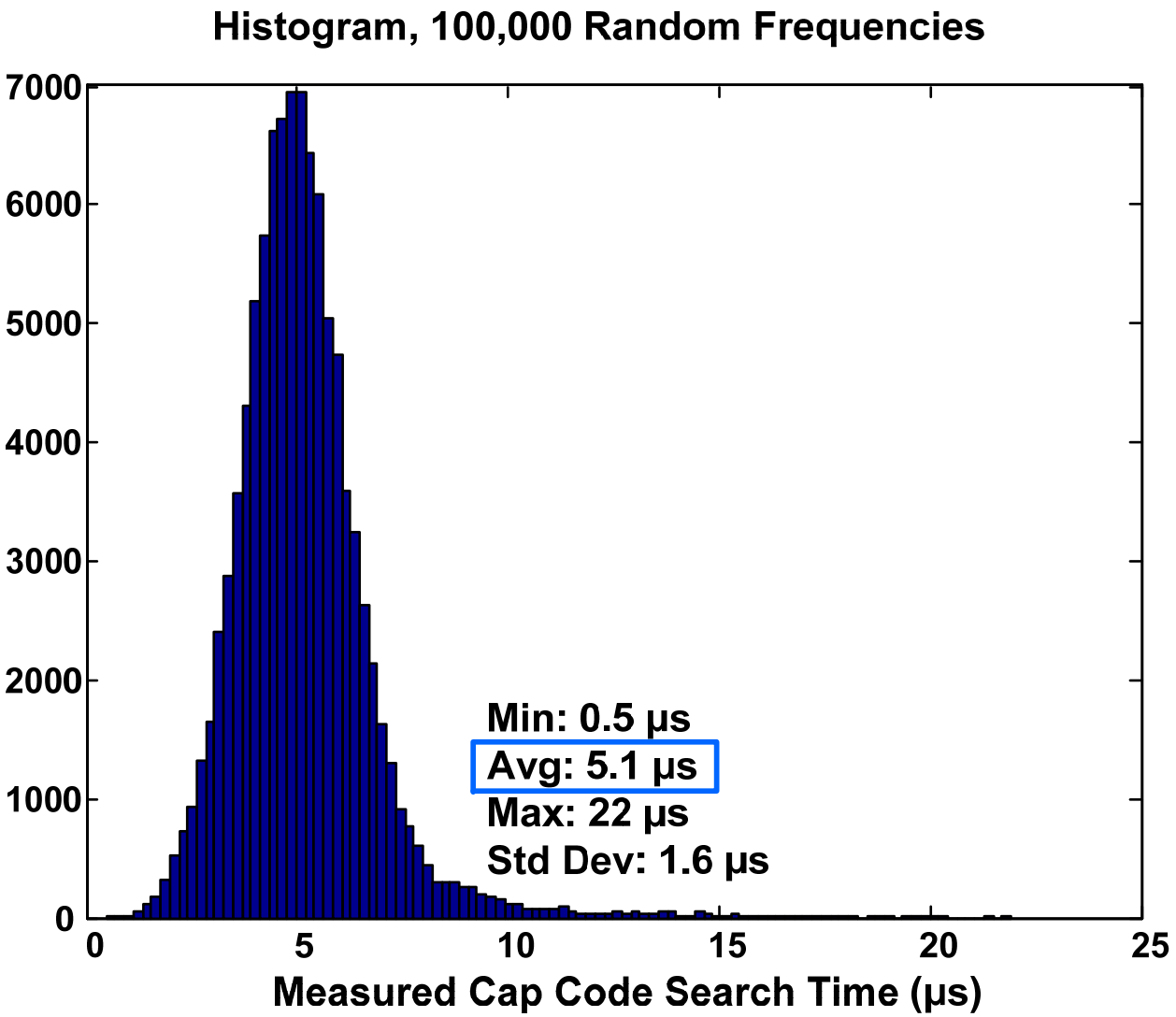
- **Gain programmability and supported BW**
  Input resistor need to vary by 7-ocatve
- **Hybrid T-network synthesis for input resistor**
  - Avoid signal attenuation for critical BW modes
  - Resistor area saving of 82%

Die Micrograph



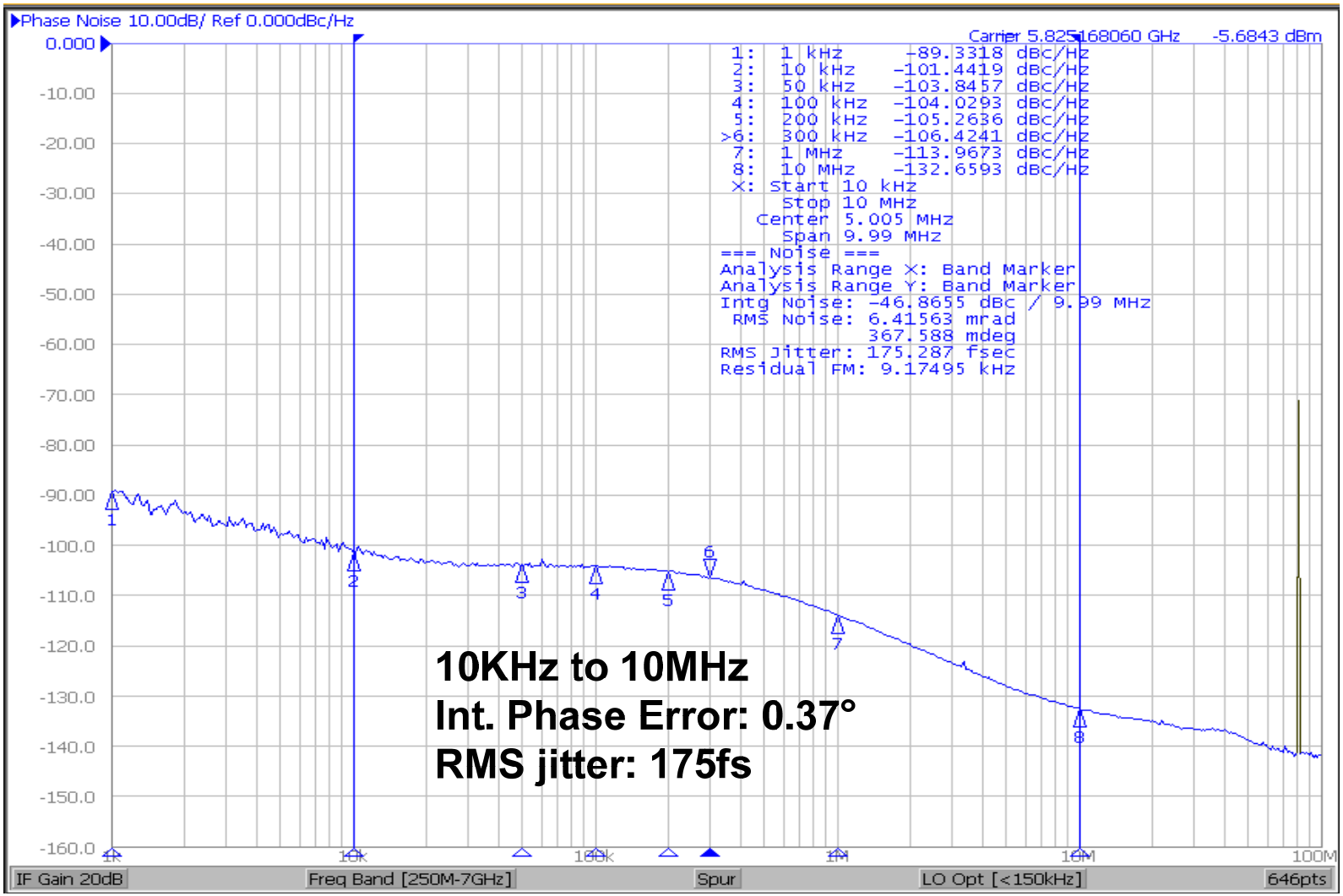
- 40nm CMOS
- 17x17 BGA package
- Die Area 46mm^2, RF/Analog 21.5mm^2

ADPLL Cap Code Search Time



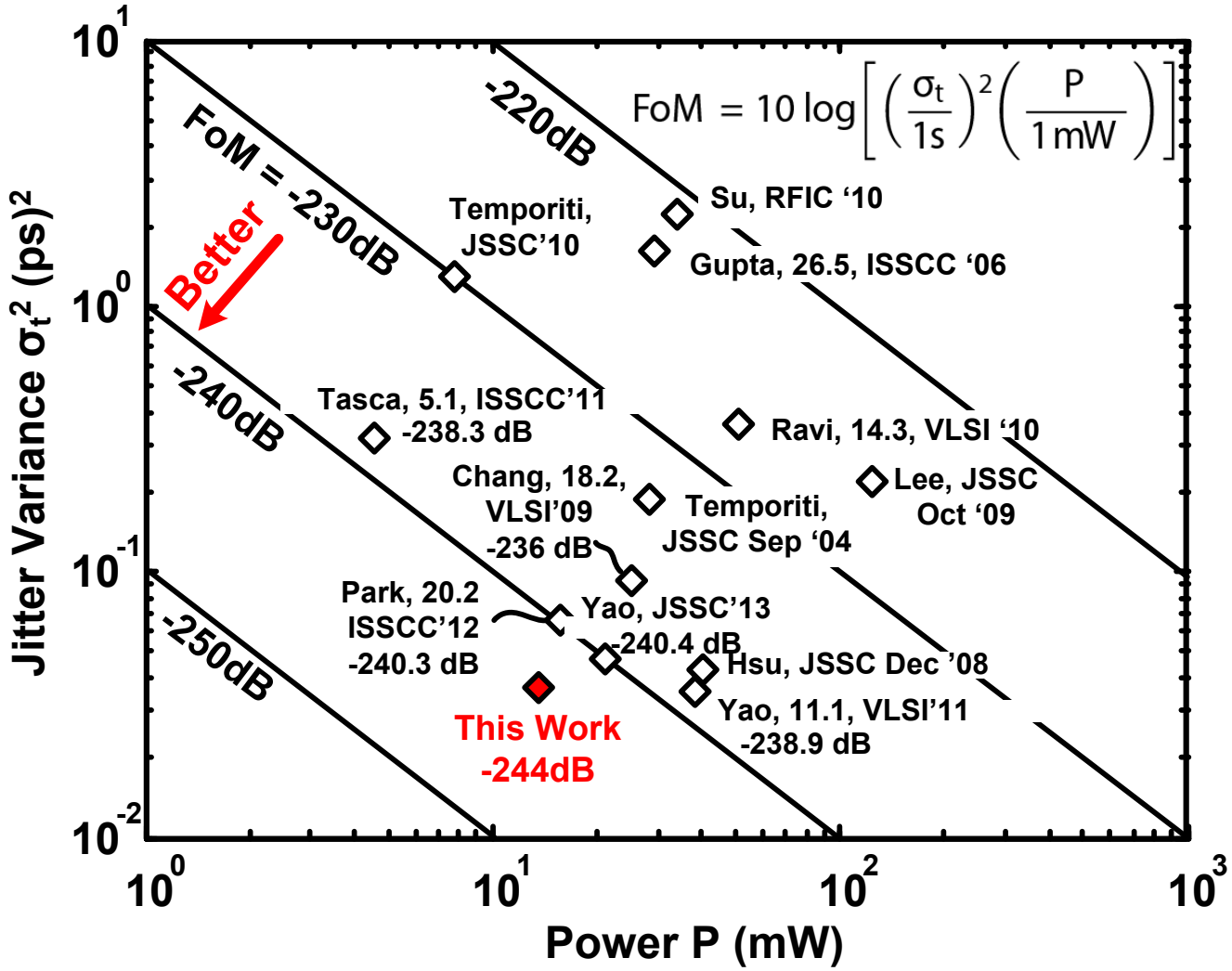
Average cap code search time = 5.1us

5.825GHz LO Phase Noise



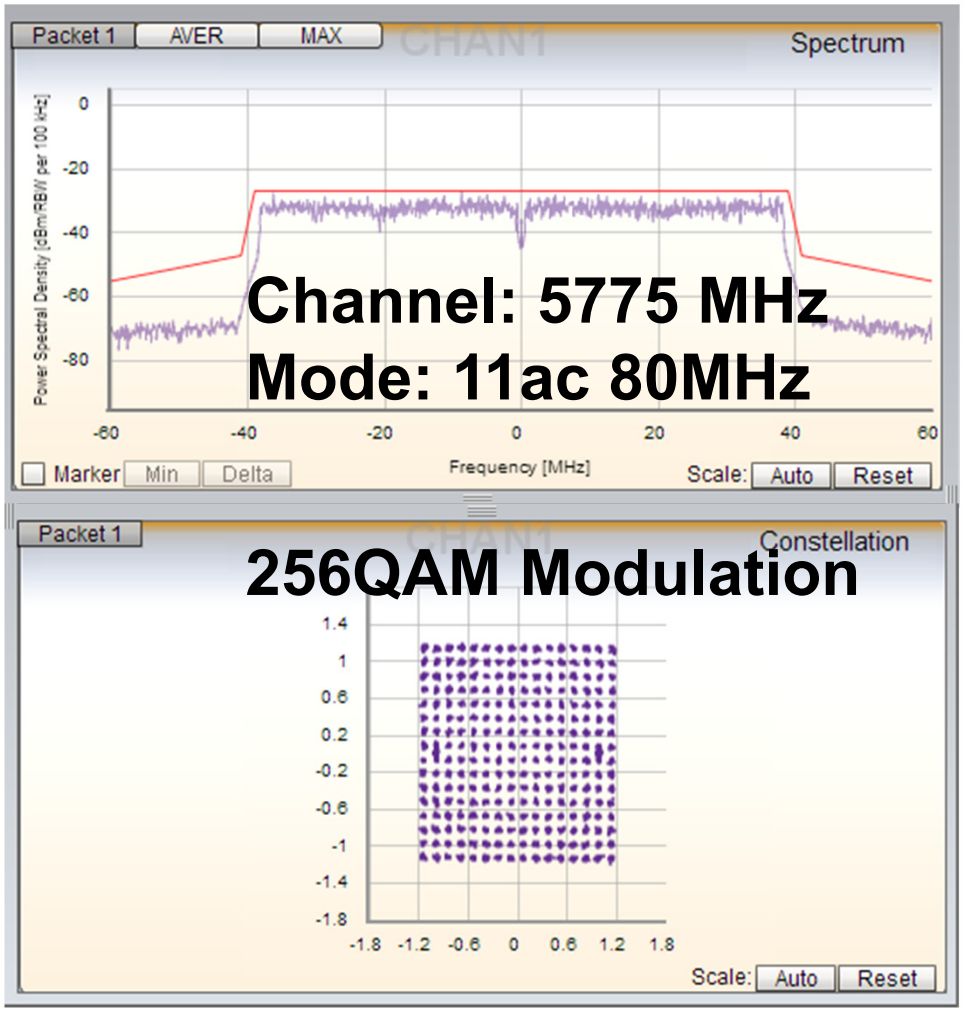
ADPLL total power consumption = 12.9mW

Frac-N PLL FoM Comparison



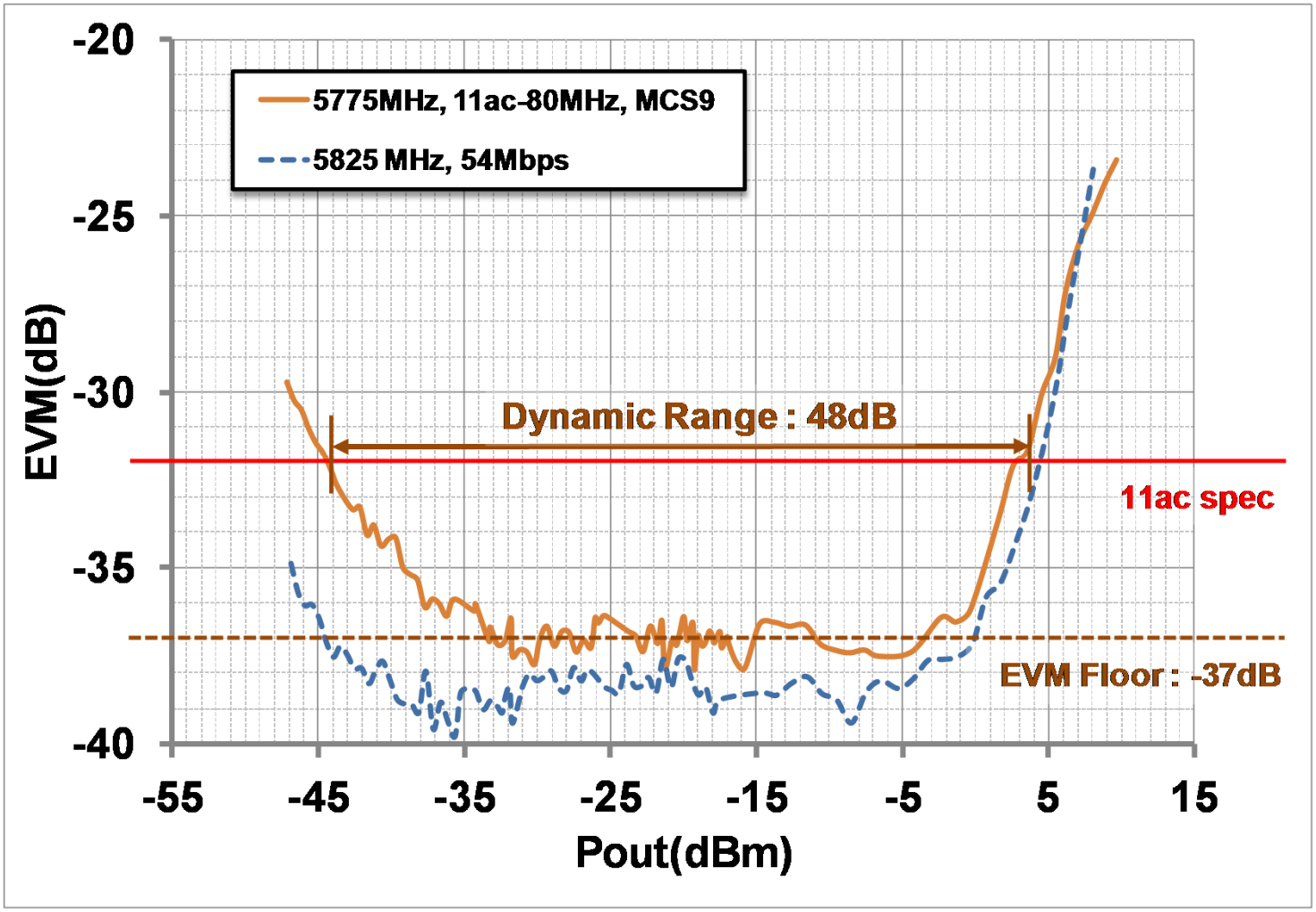
The best Frac-N PLL FoM of -244dB

5GHz TX EVM and Mask



Pout = 3dBm at EVM = -33dB

5GHz TX Dynamic Range



11ac-80M TX dynamic range = 48dB

RX ACI

Mode	IEEE spec (dBc)	Measurement (dBc)
11b	35	40
11g 54Mbps	-1	20
11a 54Mbps	-1	22
11n-40 MCS7	-2	18
11ac-80 MCS9	-9	12

Performance Summary

Integrated Phase Noise	
2.4GHz	0.19˚
5GHz	0.37˚ (at 5825MHz)
TX EVM	
2.4GHz	-41 dB @ Pout=-5dBm 802.11n, HT-40, MCS9
5GHz	-37 dB @ Pout=-5dBm 802.11ac, VHT-80, MCS9
RX Noise Figure	
2.4GHz	3 dB
5GHz	4.3 dB
Supported Signal BW	5, 10, 20, 40 and 80 MHz

Conclusions

- **A 40nm Dual-Band 3-Stream 802.11ac SoC**
  - **A Frac-N ADPLL with record FoM of -244dB**
  - **A wideband pre-PA driver with -37dB EVM floor and 48dB dynamic range for 11ac-80M**
  - **A baseband LPF supports 2.5MHz to 80MHz filter BW**

Over-the-air throughput of 1.1Gbps

Acknowledgement

- **The authors wish to thank**

  The support of the entire wireless team at Marvell, especially the DSP, software and system hardware groups

A Blocker-Resilient Wideband Receiver with Low-Noise Active Two-Point Cancellation of >0dBm TX Leakage and TX Noise in RX Band for FDD/Co-Existence

Jin Zhou, Peter R. Kinget, and Harish Krishnaswamy

CoSMIC Lab, Columbia University

New York, NY

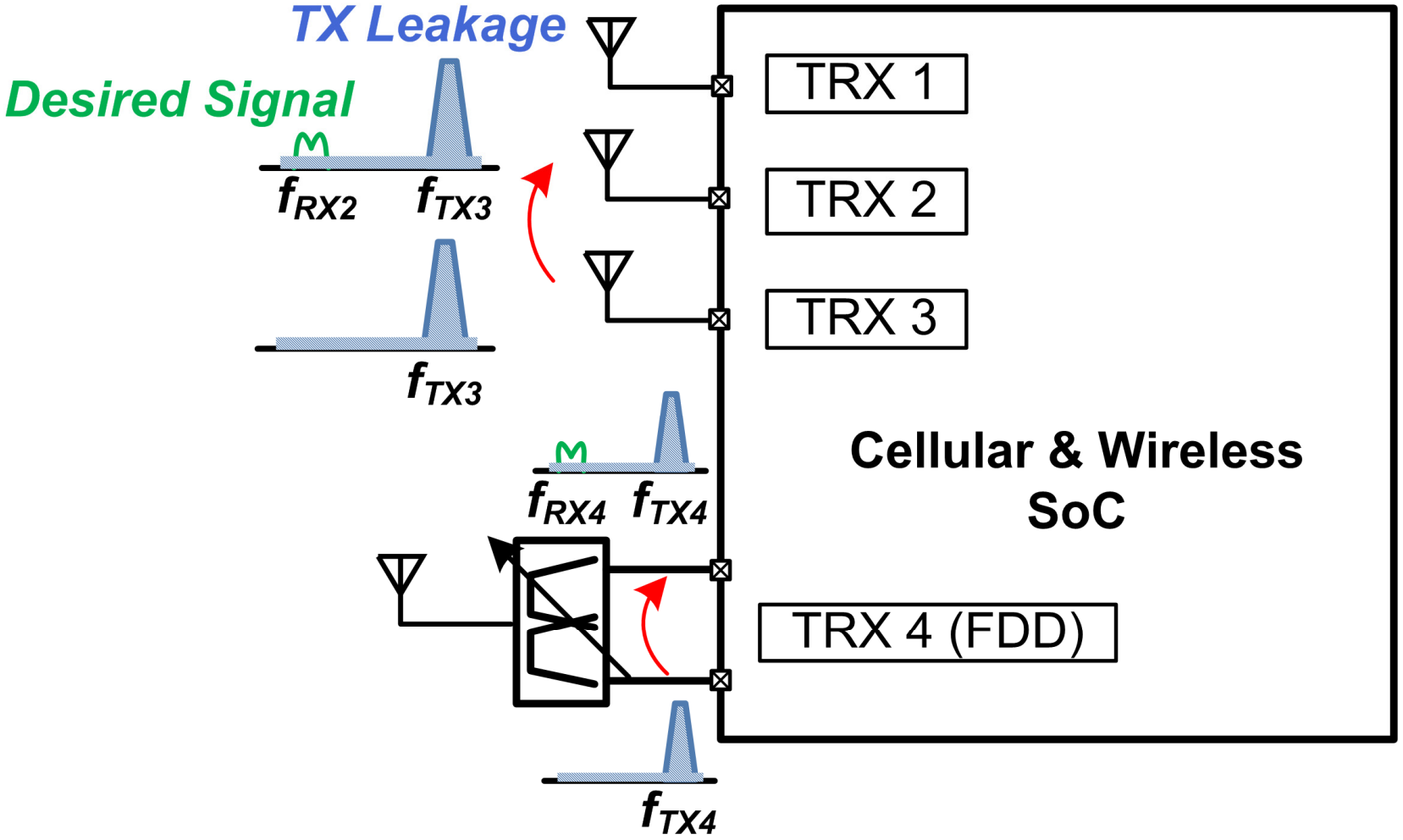
Presentation Outline

- Introduction
- Low-Noise Active Cancellation of TX Leakage and TX Noise in RX-Band
- A 65nm CMOS Implementation
- Measurement Results

Presentation Outline

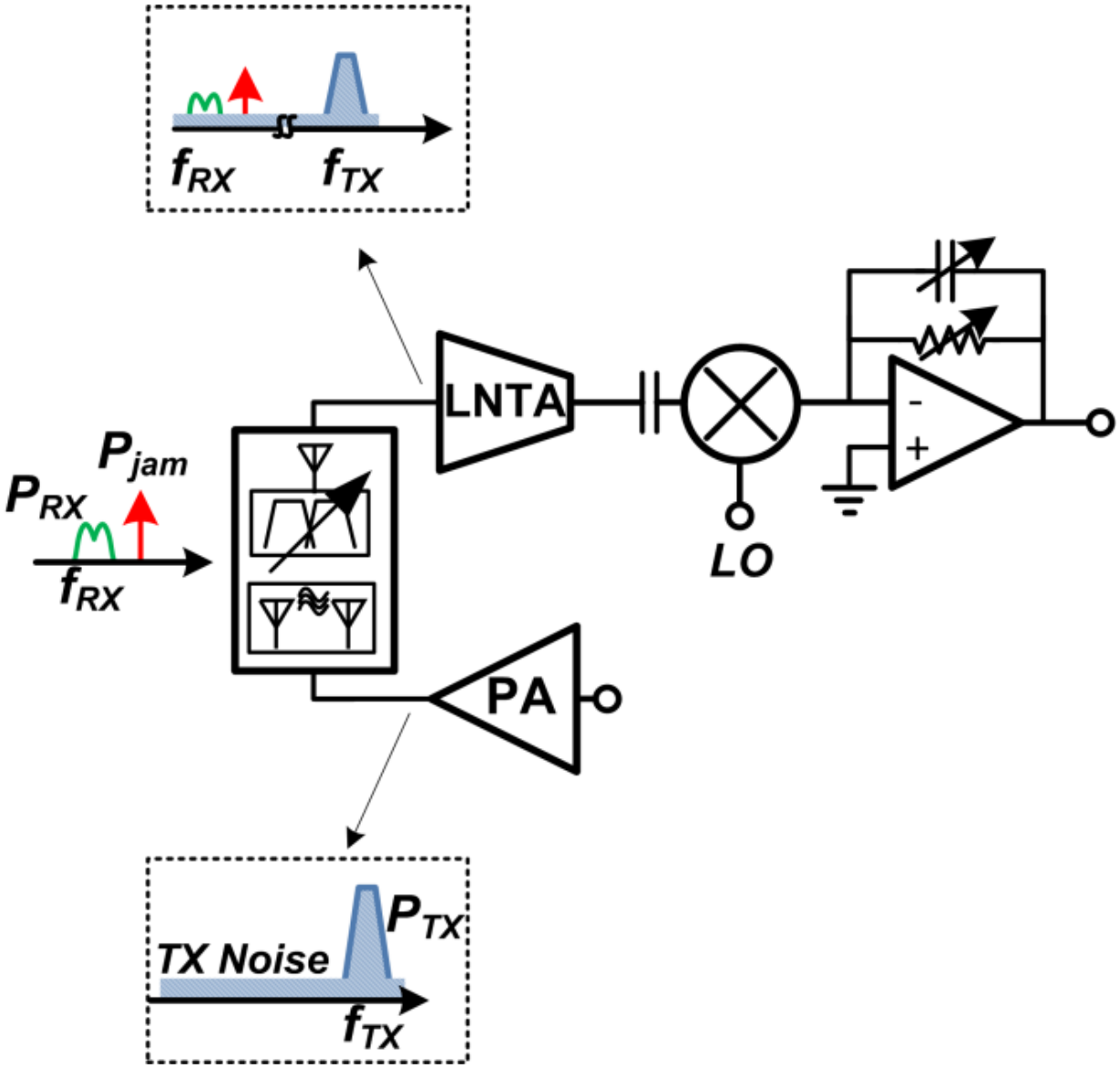
- Introduction
- Low-Noise Active Cancellation of TX Leakage and TX Noise in RX-Band
- A 65nm CMOS Implementation
- Measurement Results

Introduction

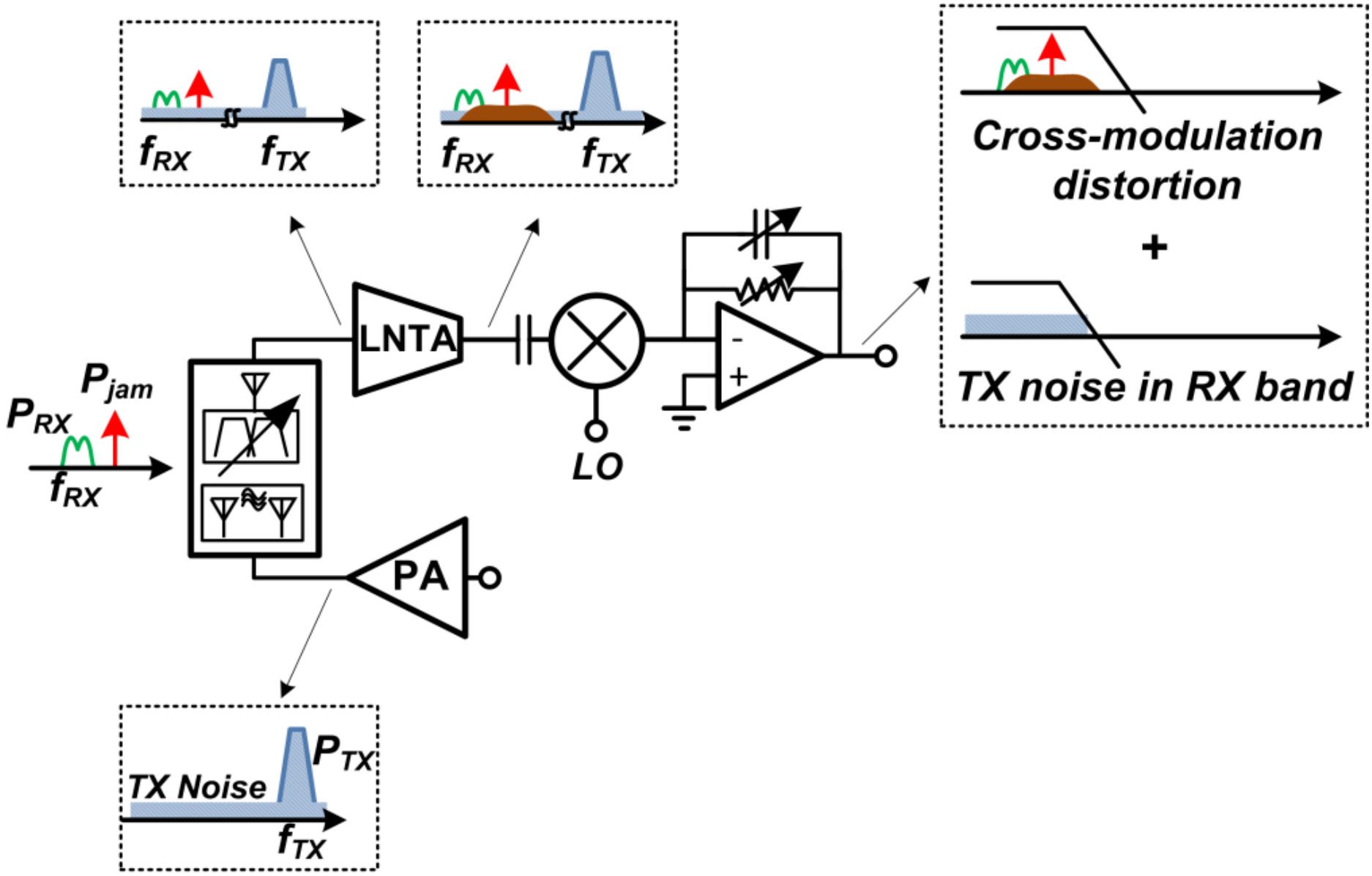


TX to RX leakage is increasing in highly integrated, reconfigurable wireless systems.

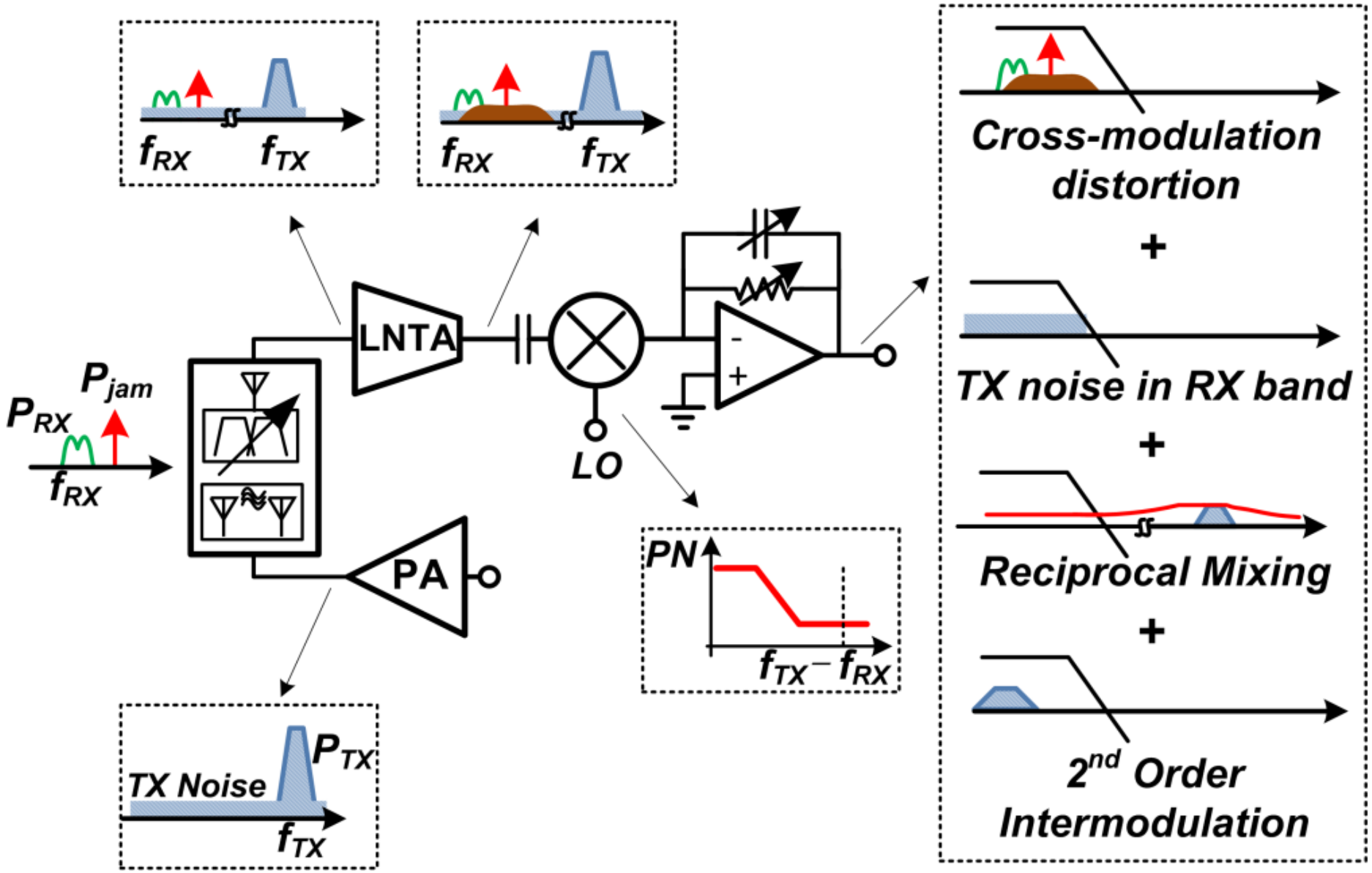
Challenges Under TX Leakage



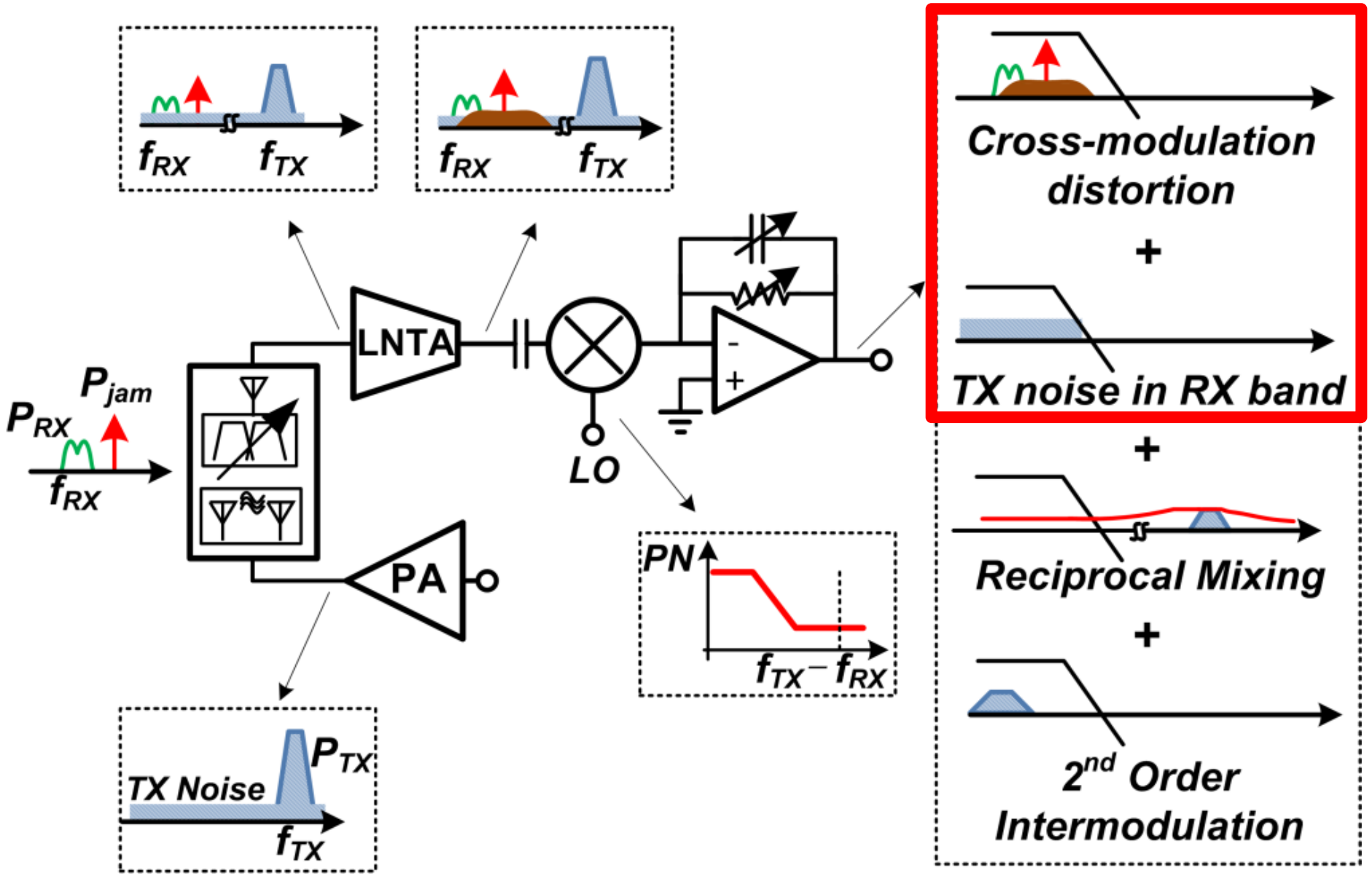
Cross Modulation and TX Noise



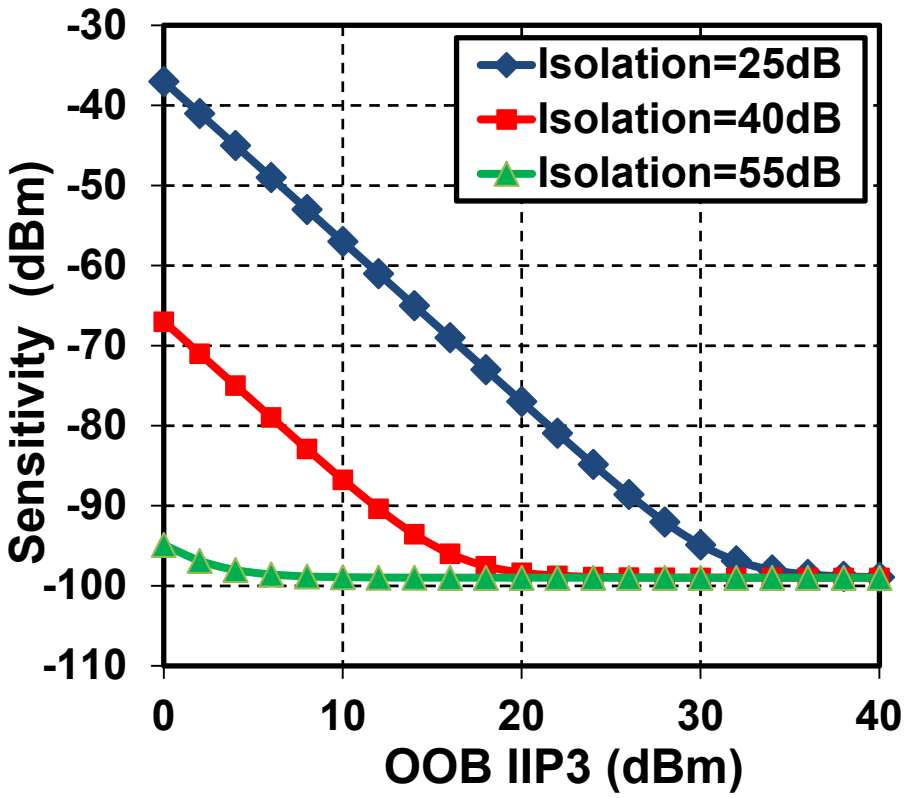
Reciprocal Mixing and IM2

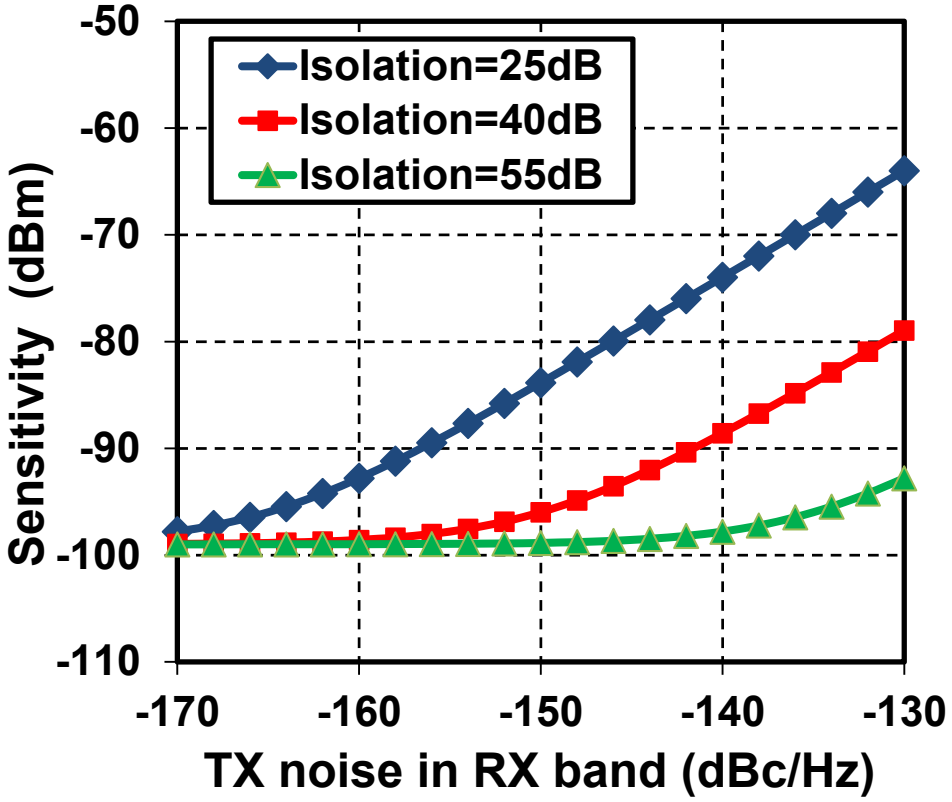


The Focus of This Work



TRX Specs Under TX Leakage

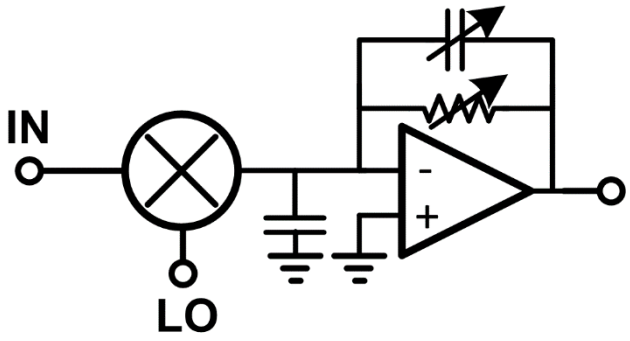
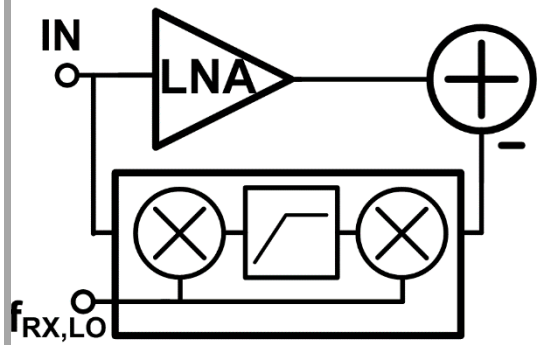
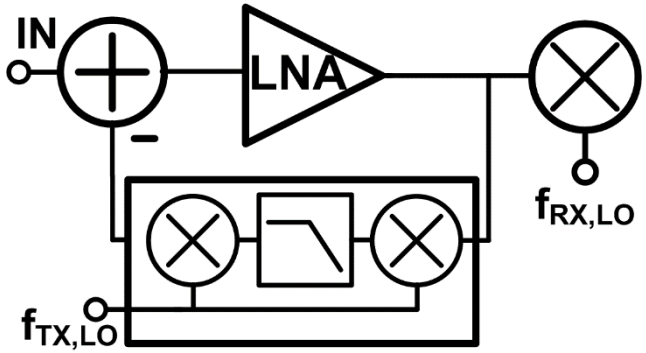




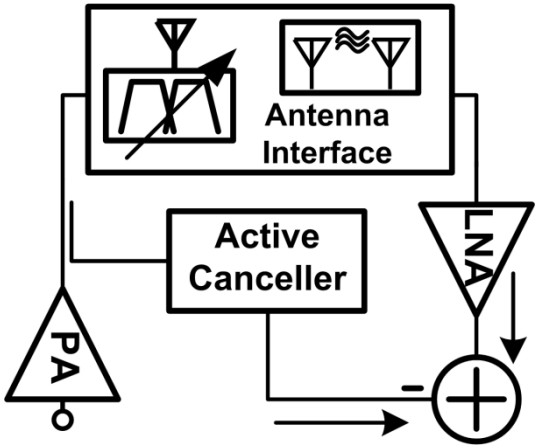
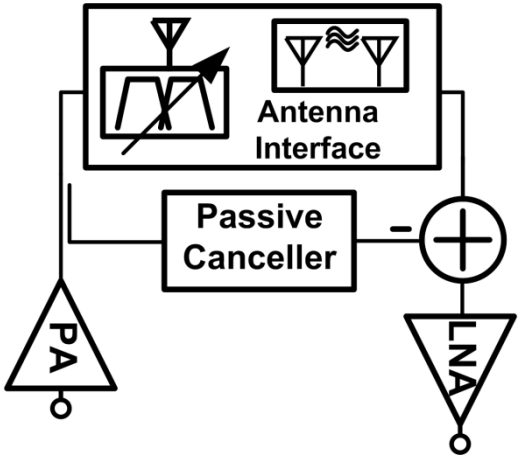
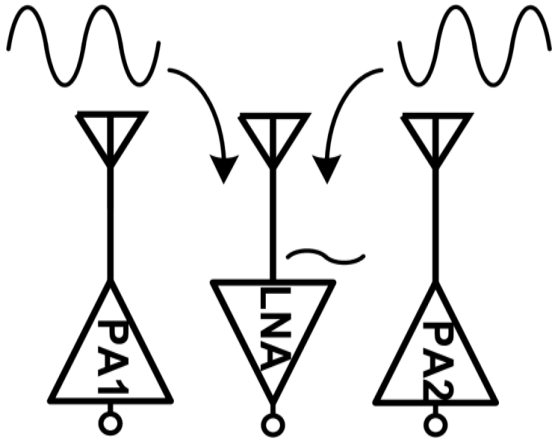
SNR: 7dB, NF: 5dB, BW: 2MHz, In-band Jammer: -30dBm, PA output Power: 21dBm

Reduced antenna/duplexer isolation imposes extremely challenging specifications for transceivers.

TX Leakage Management Techniques

Frequency-translational filtering	Feed-forward filtering	Feedback filtering
		
+ Relatively high OOB IIP3 + High linearity applies to all OOB interference - High flicker noise - LO feed through to antenna - TX noise in RX band	- Moderate NF penalty - LNA suffers from TX leakage - TX noise in RX band	+ TX leakage filtering at the LNA input - NF penalty (for high leakage levels) - Stability - TX noise in RX band

TX Leakage Management Techniques

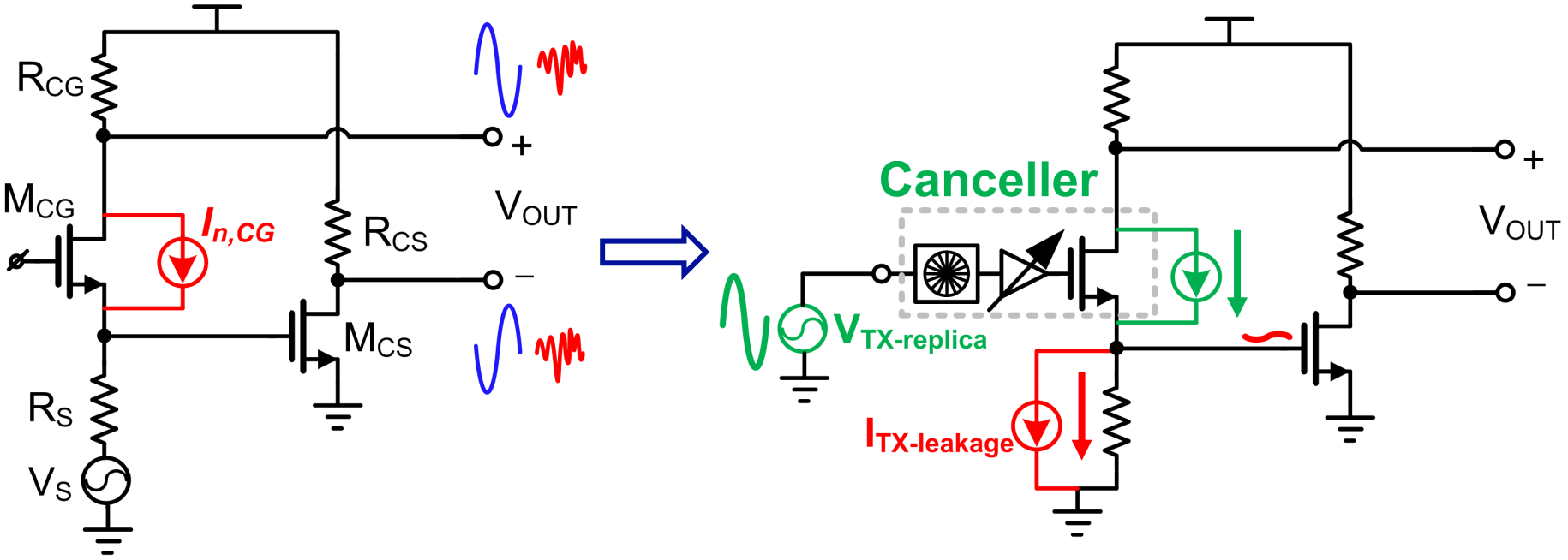
Active cancellation	Passive cancellation	Wireless cancellation
		
+ Compact, reconfigurable - Moderate NF penalty - LNA suffers from leakage - Low leakage handling	+ TX leakage cancelled at receiver input + Small NF penalty - Bulky, lack of tunability	+ TX leakage cancelled at receiver input - Multi-antenna implementation - Sensitive to EM environment - Compromised far-field radiation

New techniques for low-noise active TX leakage and TX noise cancellation are desirable.

Presentation Outline

- Introduction
- Low-Noise Active Cancellation of TX Leakage and TX Noise in RX-Band
- A 65nm CMOS Implementation
- Measurement Results

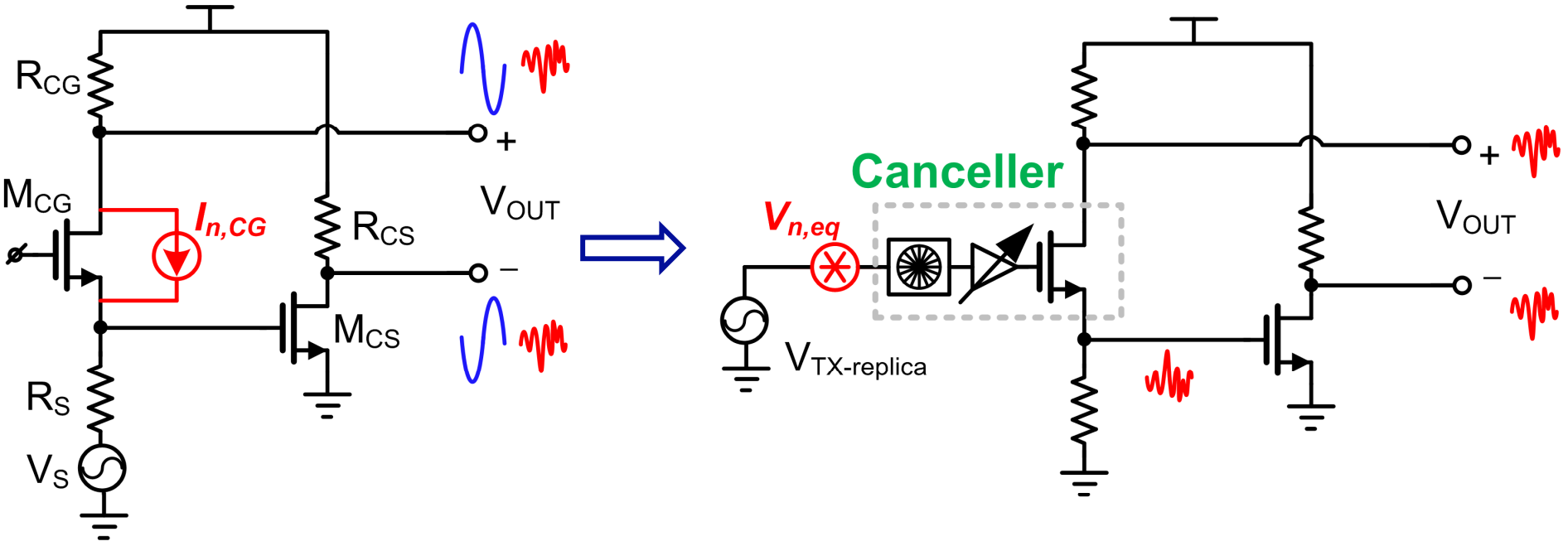
TX Leakage Cancellation in NC-LNA



[F. Bruccoleri, et al., JSSC, 2004]

NC-LNA's CG device is repurposed as part of the TX leakage canceller.

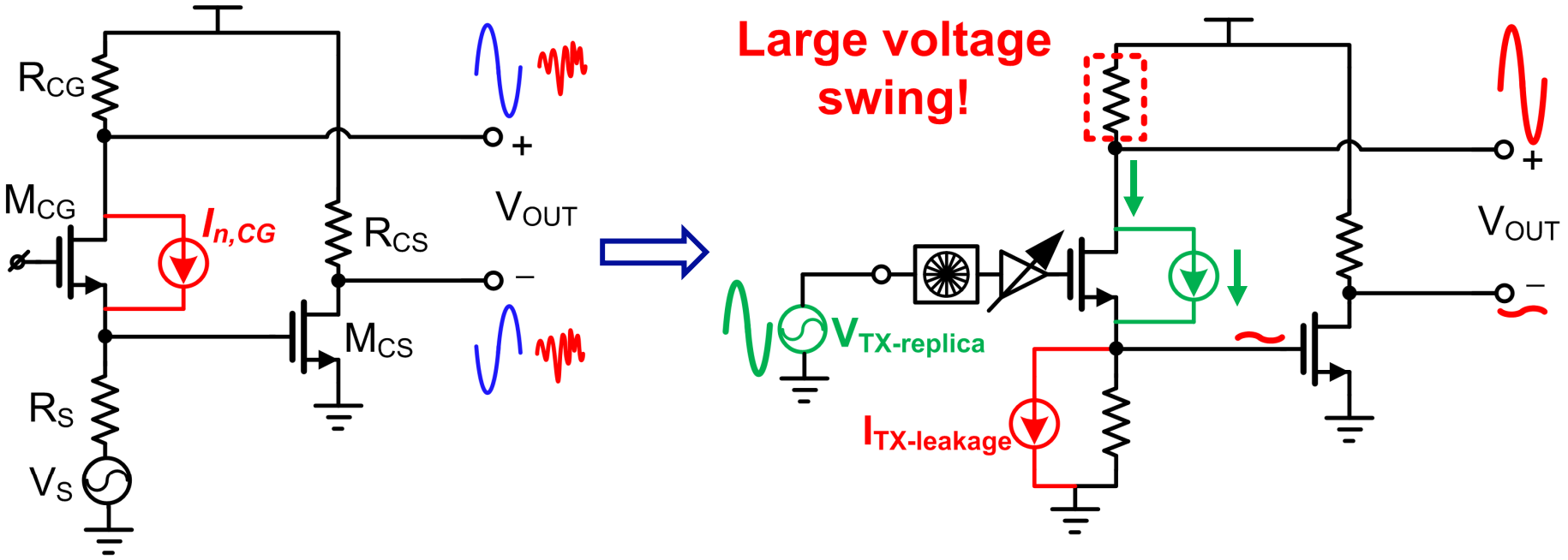
Canceller Noise Cancellation



[F. Bruccoleri, et al., JSSC, 2004]

The canceller noise is cancelled completely through the noise-cancelling property.

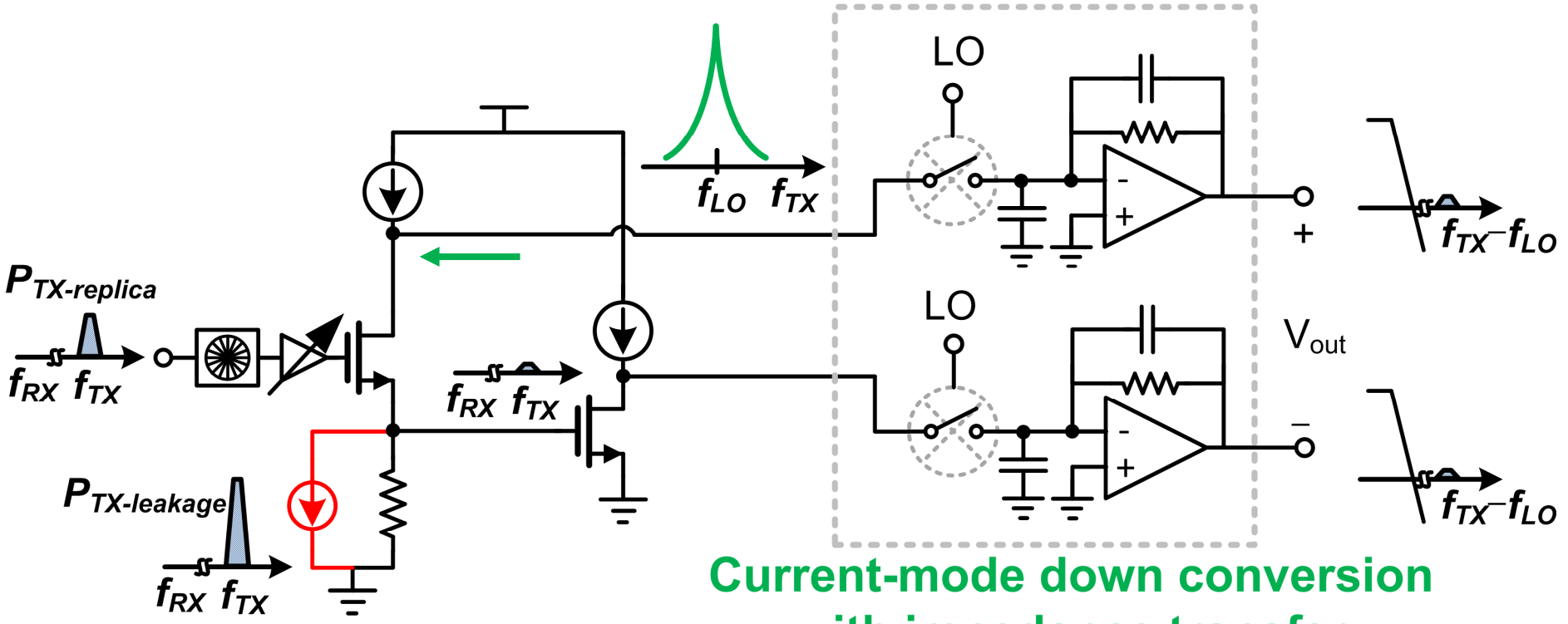
High Output Voltage Swing in CG Path



[F. Bruccoleri, et al., JSSC, 2004]

- The leakage signal remains alive at the CG output and can result in large swing in a voltage-mode LNA.

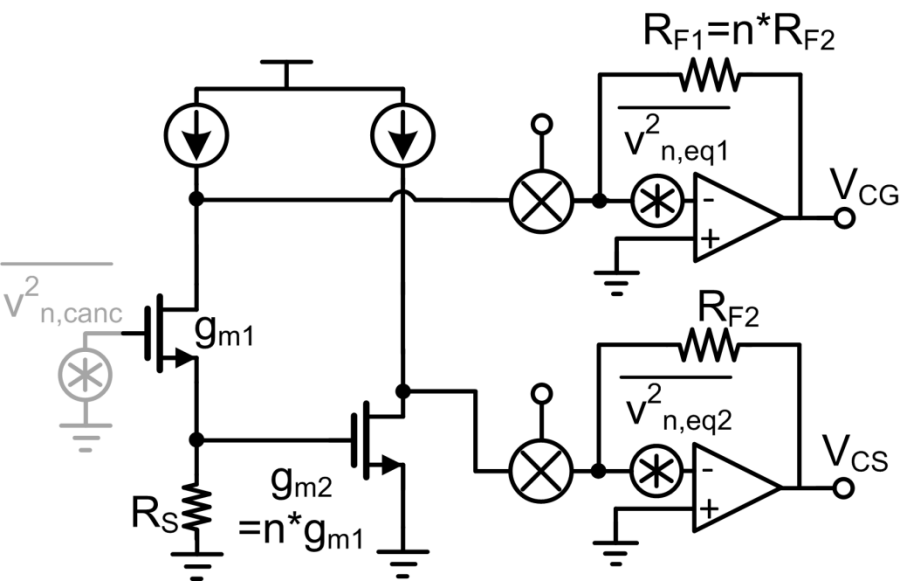
Current-Mode TX Leakage Filtering



Current-mode down conversion with impedance transfer

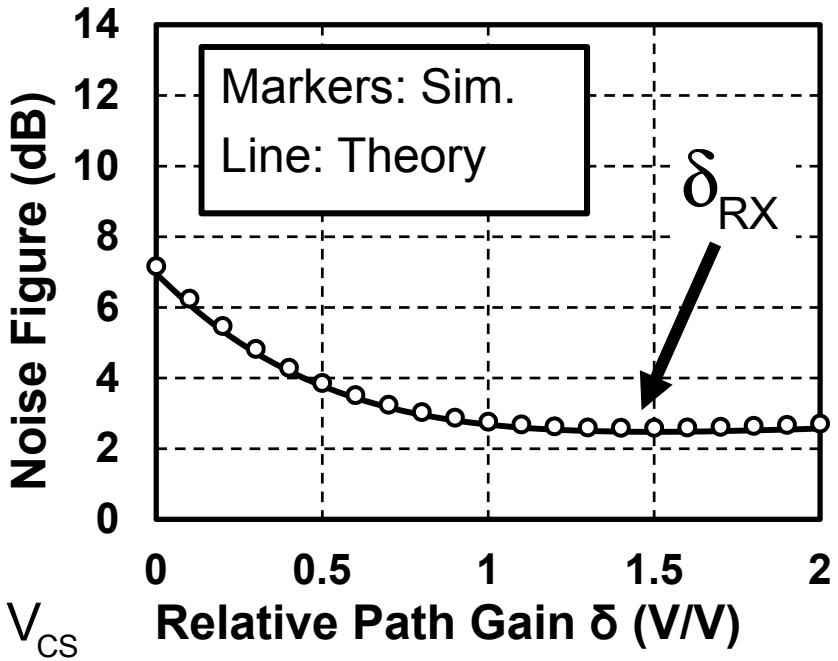
Current-mode down-conversion is used to filter out the CG-path TX leakage without linearity issues.

RX Noise Figure



4-phase mixing is not shown for simplicity

$$V_{OUT} = \delta V_{CG} - V_{CS}$$

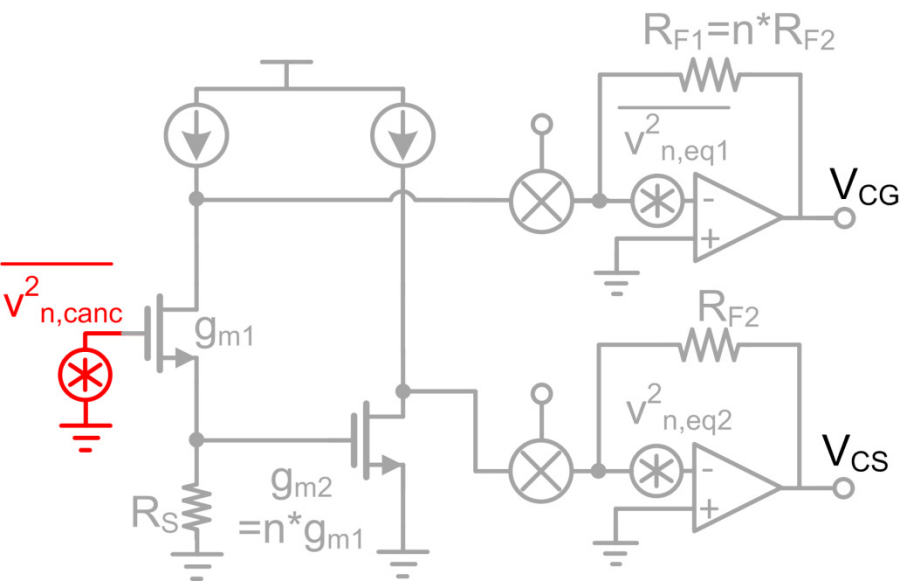


CG Device + CG Canceller Noise ***LNTA CS Device Noise*** ***TIA Noise***

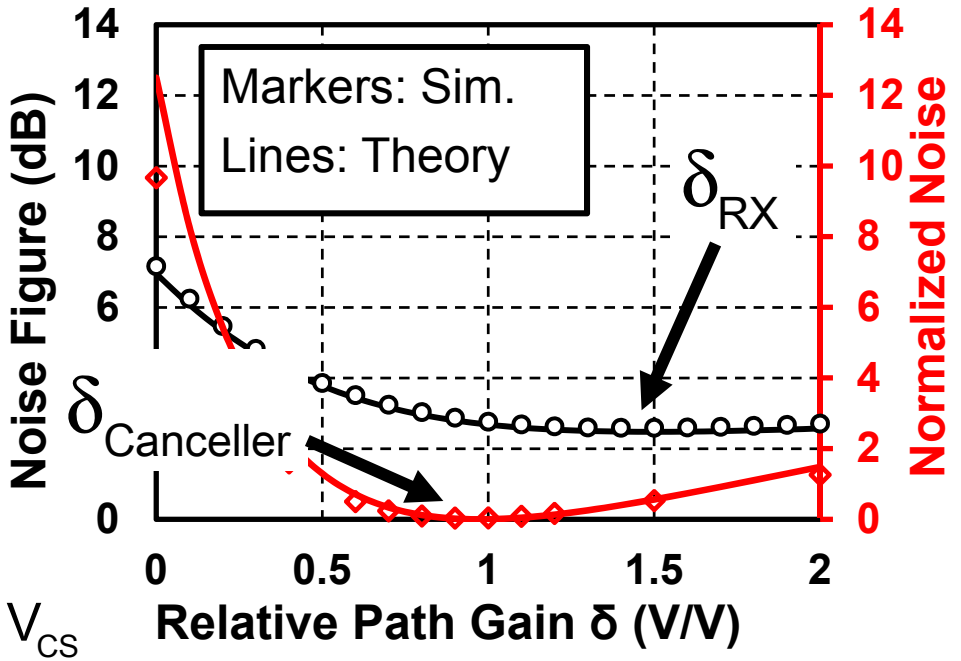
$$F = K_{Fold}\left\{1+\frac{\left(R_{F1}\delta - R_S g_{m2} R_{F2}\right)^2\left(\gamma g_{m1} + \overline{v^2_{n,canc}}\frac{g^2_{m1}}{4kT}\right) + R^2_{F2}\gamma g_{m2}\left(1+g_{m1}R_S\right)^2}{\left(g_{m1}R_{F1}\delta + g_{m2}R_{F2}\right)^2 R_S}\right\} + \pi^2\frac{\left(1+g_{m1}R_S\right)^2\left(\overline{v^2_{n,eq1}}\delta^2 + \overline{v^2_{n,eq2}}\right)}{\left(g_{m1}R_{F1}\delta + g_{m2}R_{F2}\right)^2 R_S}$$

For the RX without the CG canceller, optimum relative gain for NF is δ>1.

Excess Noise of the CG Canceller



4-phase mixing is not shown for simplicity



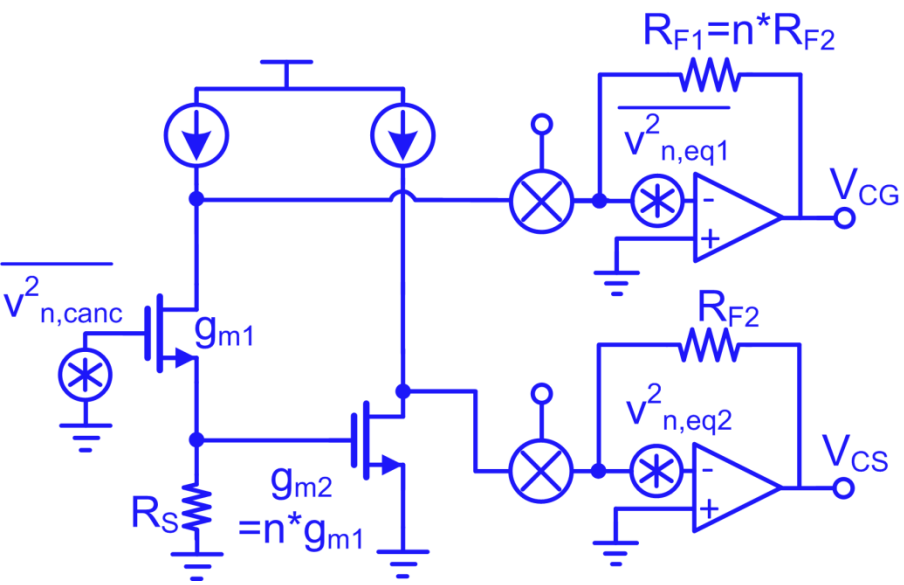
$$V_{OUT} = \delta V_{CG} - V_{CS}$$

CG Device + CG Canceller Noise ***LNTA CS Device Noise*** ***TIA Noise***

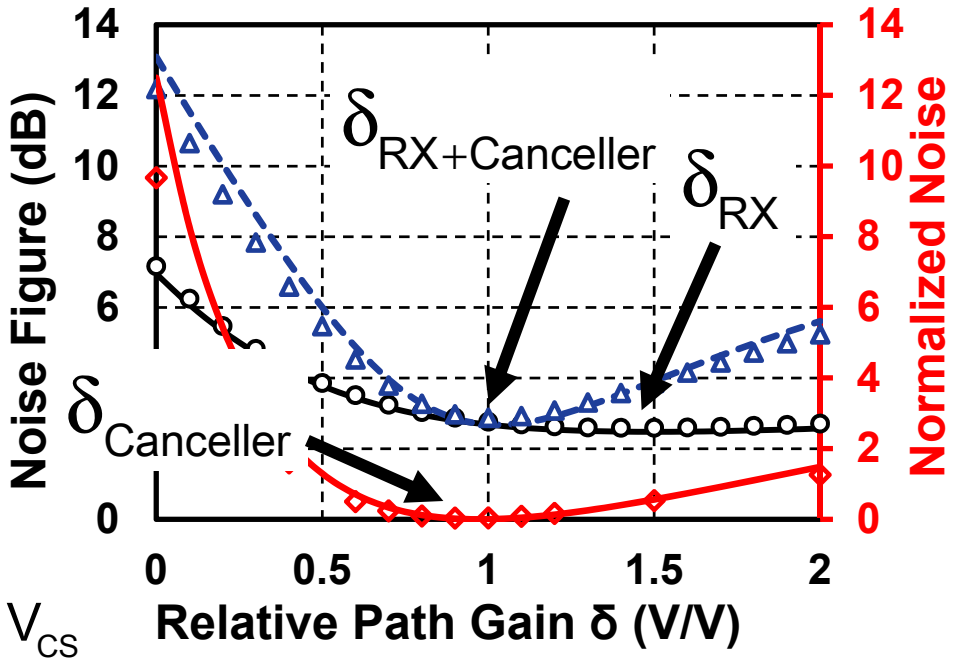
$$F = K_{Fold}\left\{1+\frac{\left(R_{F1}\delta - R_S g_{m2} R_{F2}\right)^2\left(\gamma g_{m1} + \overline{v^2_{n,canc}}\frac{g^2_{m1}}{4kT}\right) + R^2_{F2}\gamma g_{m2}\left(1+g_{m1}R_S\right)^2}{\left(g_{m1}R_{F1}\delta + g_{m2}R_{F2}\right)^2 R_S}\right\} + \pi^2\frac{\left(1+g_{m1}R_S\right)^2\left(\overline{v^2_{n,eq1}}\delta^2 + \overline{v^2_{n,eq2}}\right)}{\left(g_{m1}R_{F1}\delta + g_{m2}R_{F2}\right)^2 R_S}$$

For the CG canceller noise, the optimum relative path gain for NF is δ=1.

Overall TX Leakage Cancelling RX NF



4-phase mixing is not shown for simplicity



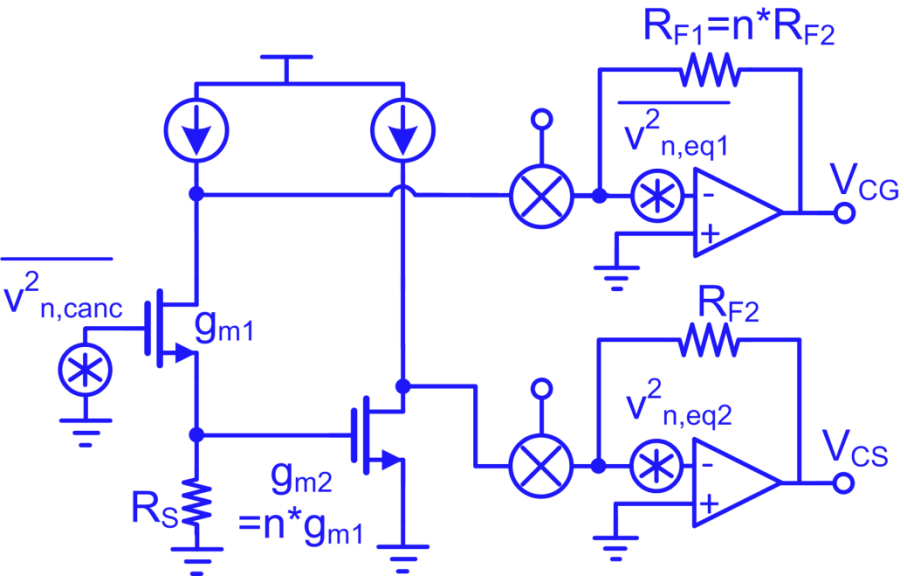
$$V_{OUT} = \delta V_{CG} - V_{CS}$$

CG Device + CG Canceller Noise ***LNTA CS Device Noise*** ***TIA Noise***

$$F = K_{Fold}\left\{1 + \frac{\left(R_{F1}\delta - R_S g_{m2} R_{F2}\right)^2 \left(\gamma g_{m1} + \overline{v^2_{n,canc}}\frac{g^2_{m1}}{4kT}\right) + R^2_{F2}\gamma g_{m2}\left(1 + g_{m1}R_S\right)^2}{\left(g_{m1}R_{F1}\delta + g_{m2}R_{F2}\right)^2 R_S}\right\} + \pi^2 \frac{\left(1 + g_{m1}R_S\right)^2 \left(\overline{v^2_{n,eq1}}\delta^2 + \overline{v^2_{n,eq2}}\right)}{\left(g_{m1}R_{F1}\delta + g_{m2}R_{F2}\right)^2 R_S}$$

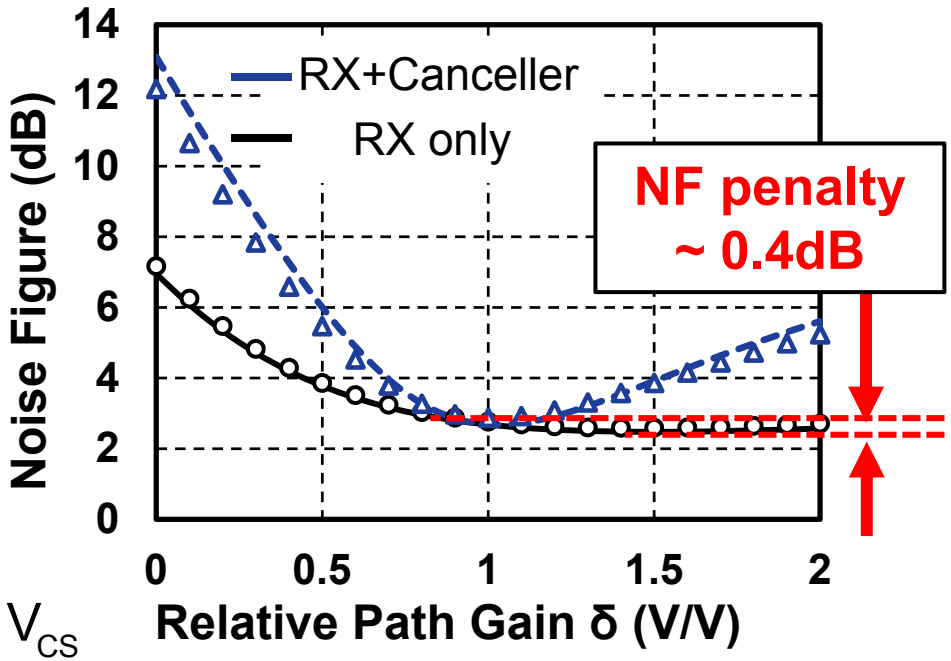
For RX with CG canceller active, the optimum relative path gain for NF approaches 1 as the canceller noise dominates.

Resultant NF Penalty



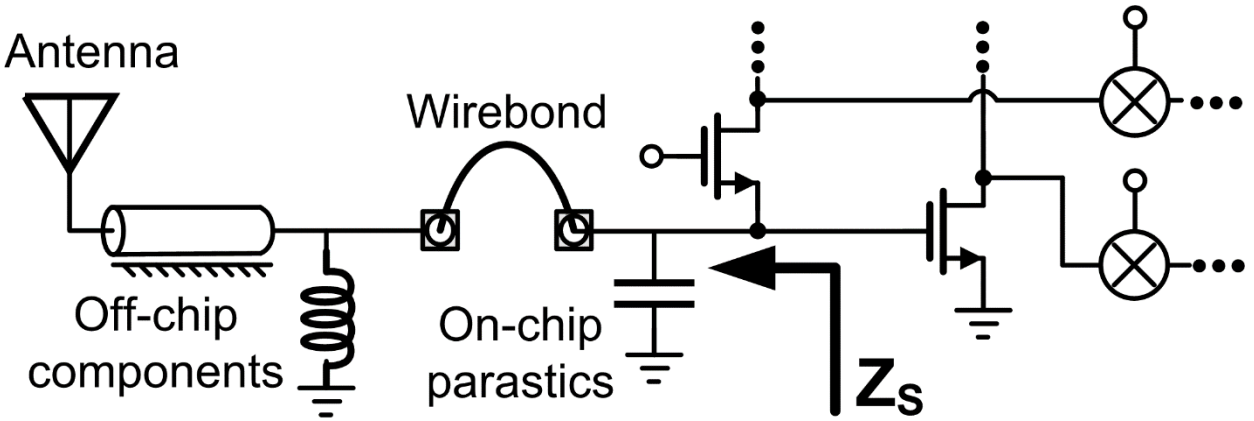
4-phase mixing is not shown for simplicity

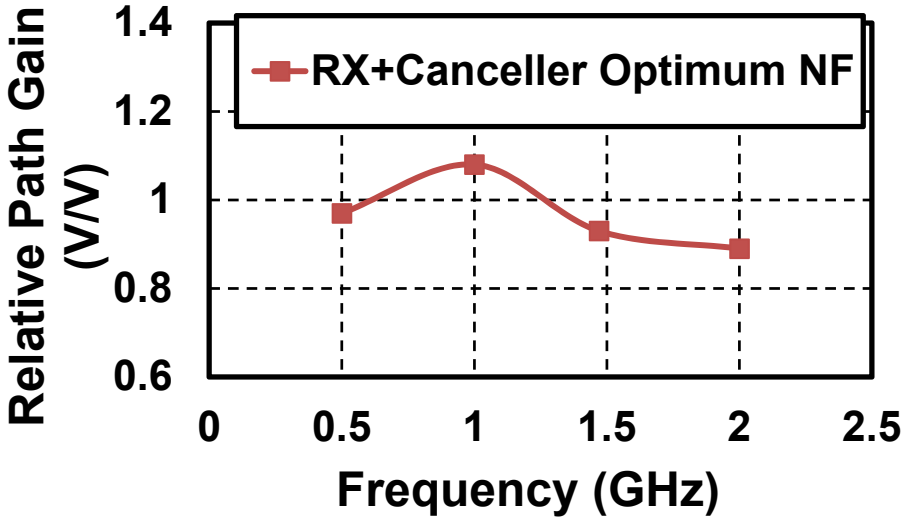
$$V_{OUT} = \delta V_{CG} - V_{CS}$$

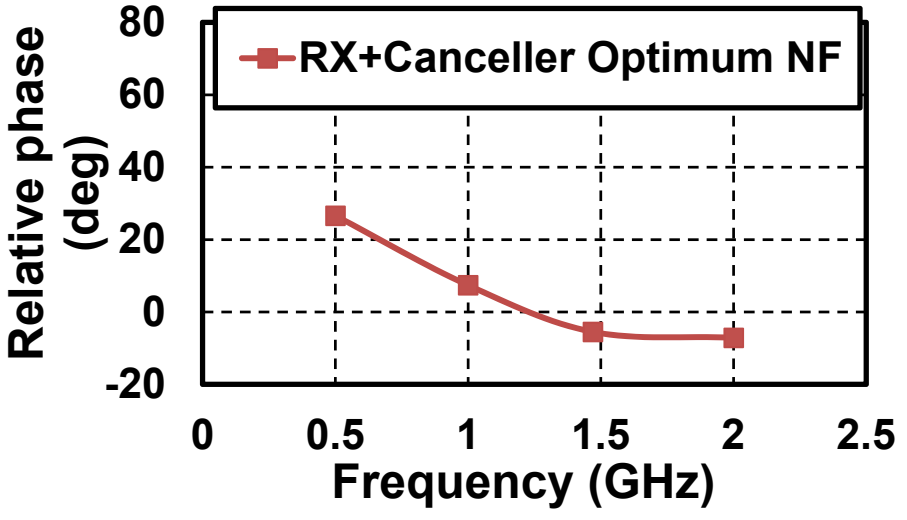


Resultant NF penalty is small (~0.4dB in sim.).

Optimum NF Condition with Varying Z_S

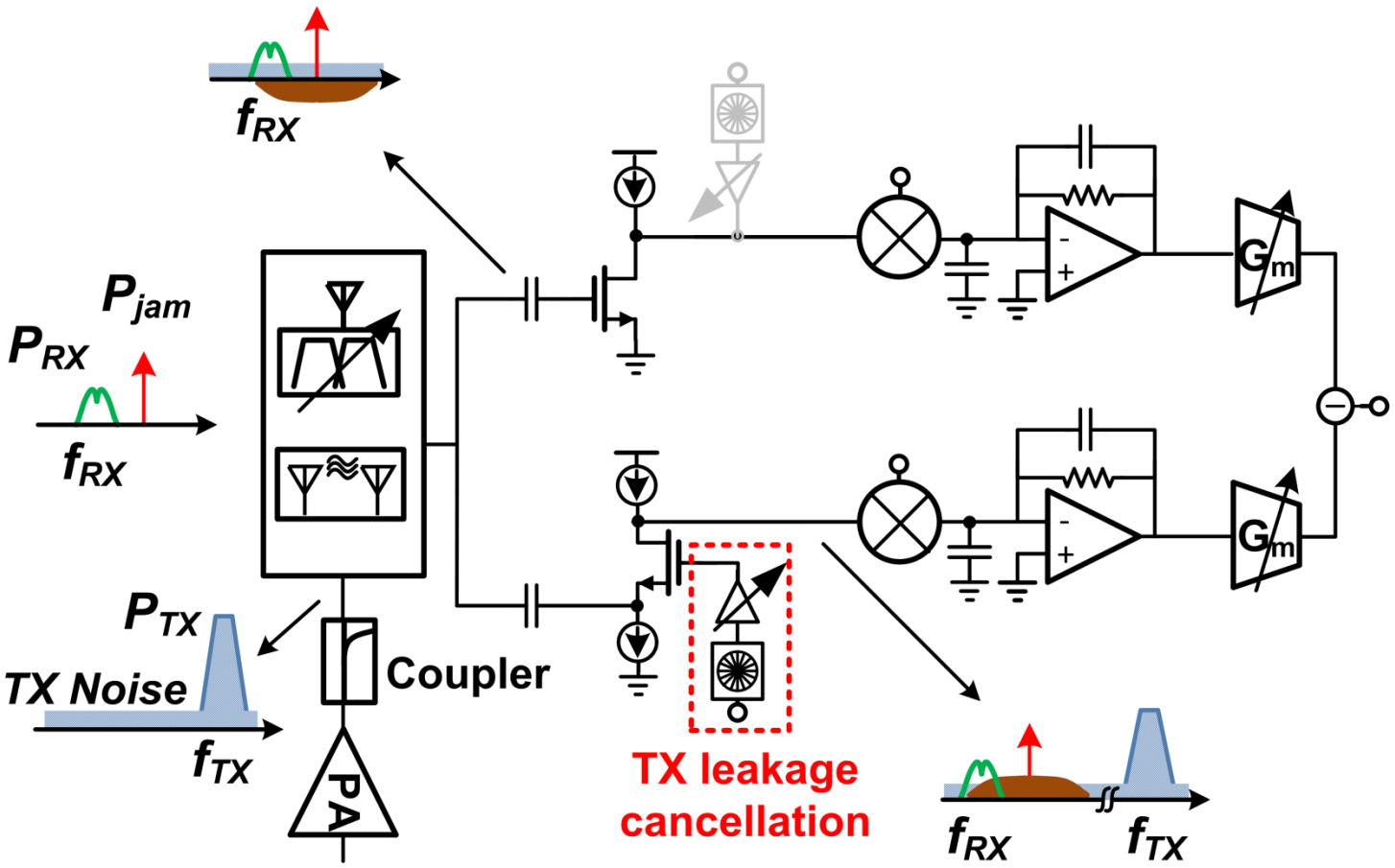






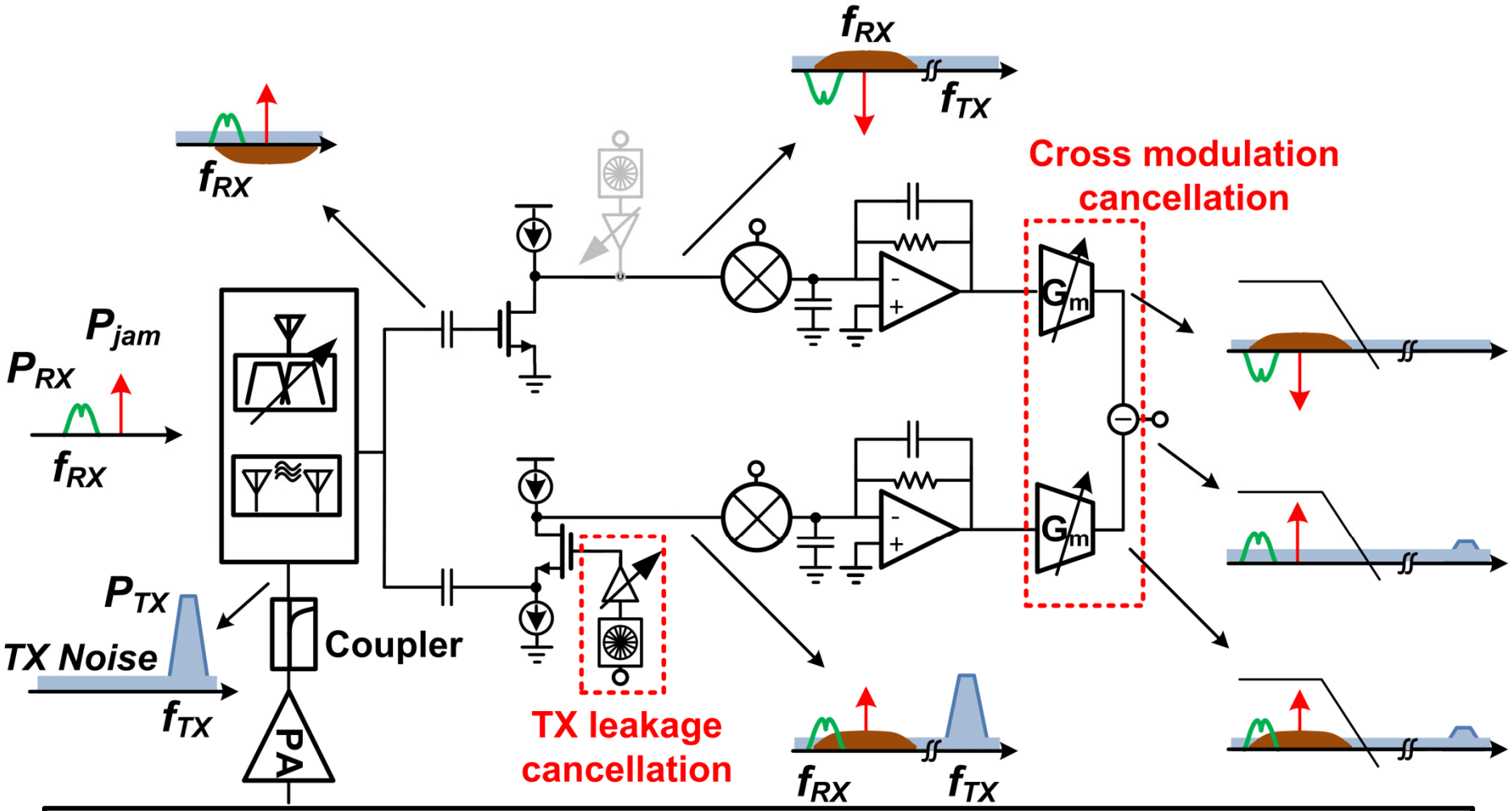
With package parasitics and off-chip biasing components, optimum relative gain is ~1 with 10% variation with a phase that varies from 30° to -10°.

Cross Modulation in the CG Device



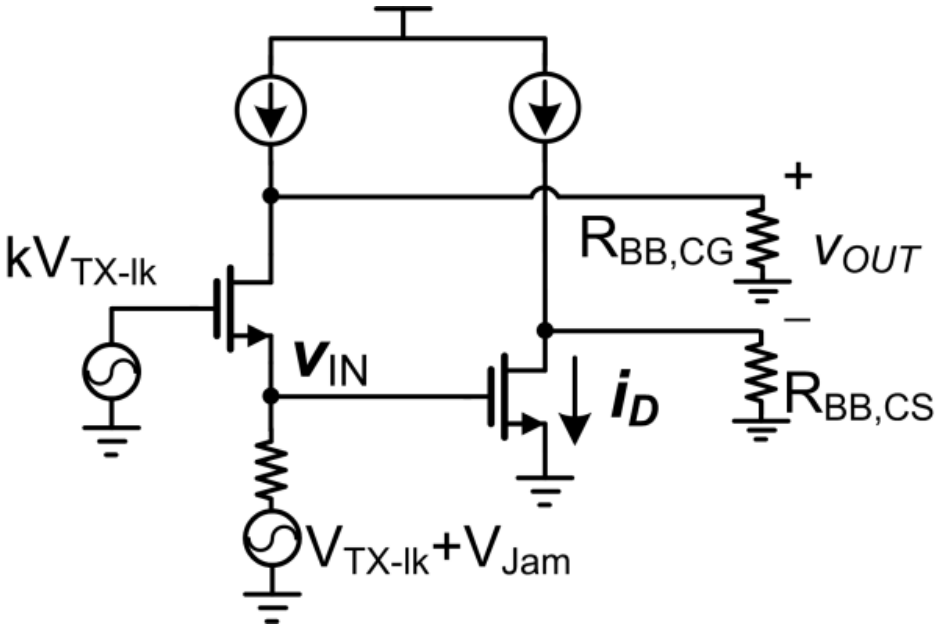
- TX leakage is cancelled at the RX input, but the CG device sees large leakage swings and generates cross-modulation products.

Cross Mod. Distortion Cancellation



Cross-modulation products are cancelled through the distortion cancellation property of noise canceling.

Modeling LNTA Nonlinearity



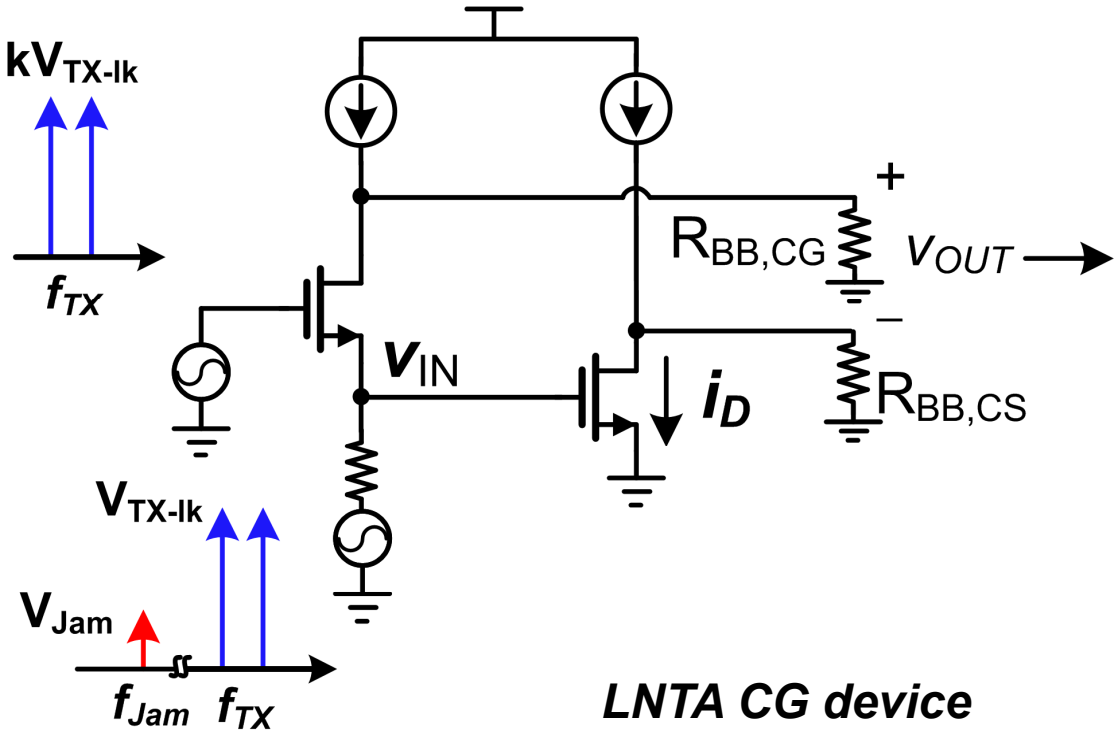
Expand the input voltage v_{IN} as:

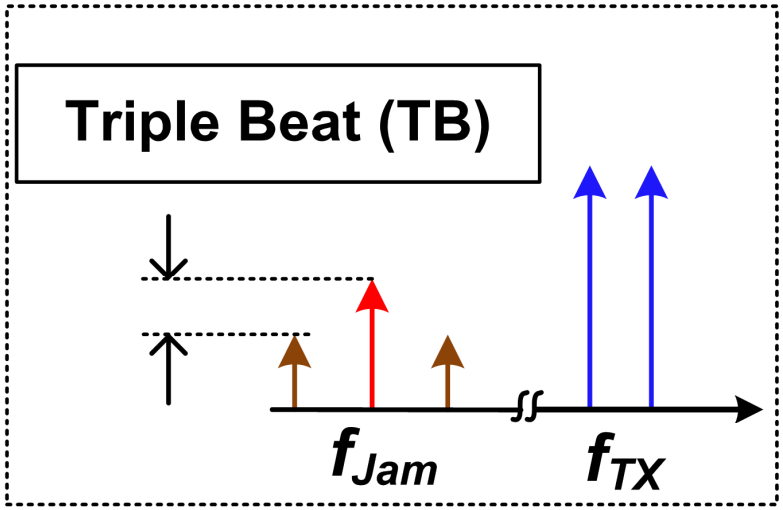
$$v_{IN} = \alpha_{1T} v_{TX-lk} + \alpha_{2T} v^2_{TX-lk} + \alpha_{3T} v^3_{TX-lk} + \alpha_{1S} v_{Jam} + \alpha_{2S} v^2_{Jam} + \alpha_{3S} v^3_{Jam}$$
$$+ \alpha_{2TS} v_{TX-lk} v_{Jam} + \alpha_{3T^2S} v^2_{TX-lk} v_{Jam} + \alpha_{3TS^2} v_{TX-lk} v^2_{Jam}$$

Expand the CS device drain current i_D as:

$$i_D = g_{m2} v_{IN} + \frac{1}{2} g'_{m2} v^2_{IN} \frac{1}{6} g''_{m2} v^3_{IN}$$

Cross Modulation Distortion Analysis





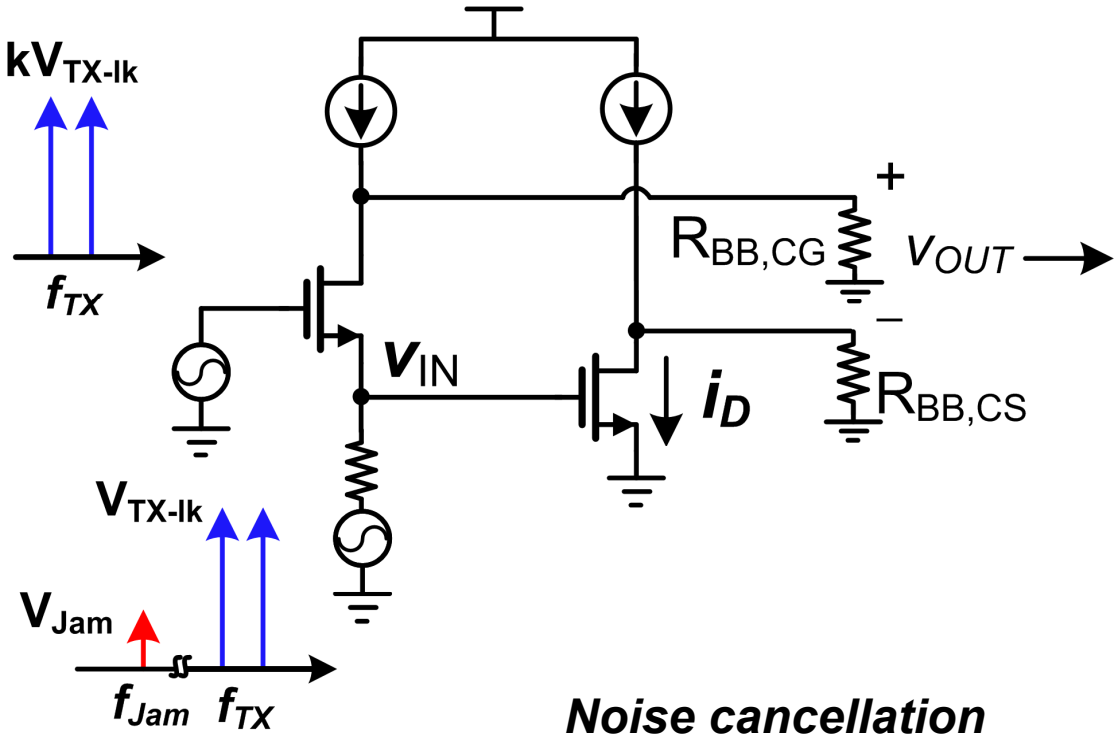
LNTA CG device 3rd order distortion

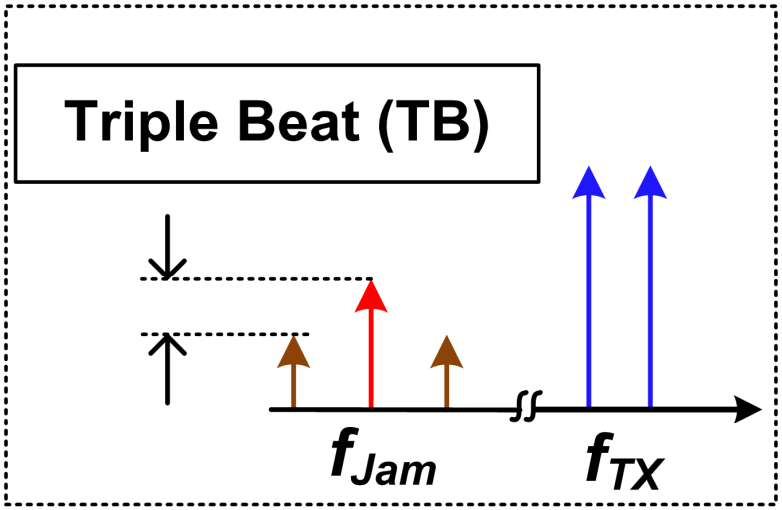
LNTA CS device 3rd order distortion

$$TB^{-1} \equiv \frac{\text{Cross-mod. Dist.}}{\text{In-band Jammer}} \propto \left(g_{m2} R_S - \frac{R_{BB,CG}}{R_{BB,CS}} \right) \alpha_{3T^2S} + \left[g'_{m2} \left(\alpha_{2T} + \alpha_{2TS} \alpha_{1T} \right) + \frac{1}{2} g''_{m2} \alpha^2_{1T} \right] \frac{R_S}{2}$$

Interaction between 2nd order distortion of CG and CS devices

Cross Mod. Distortion Cancellation





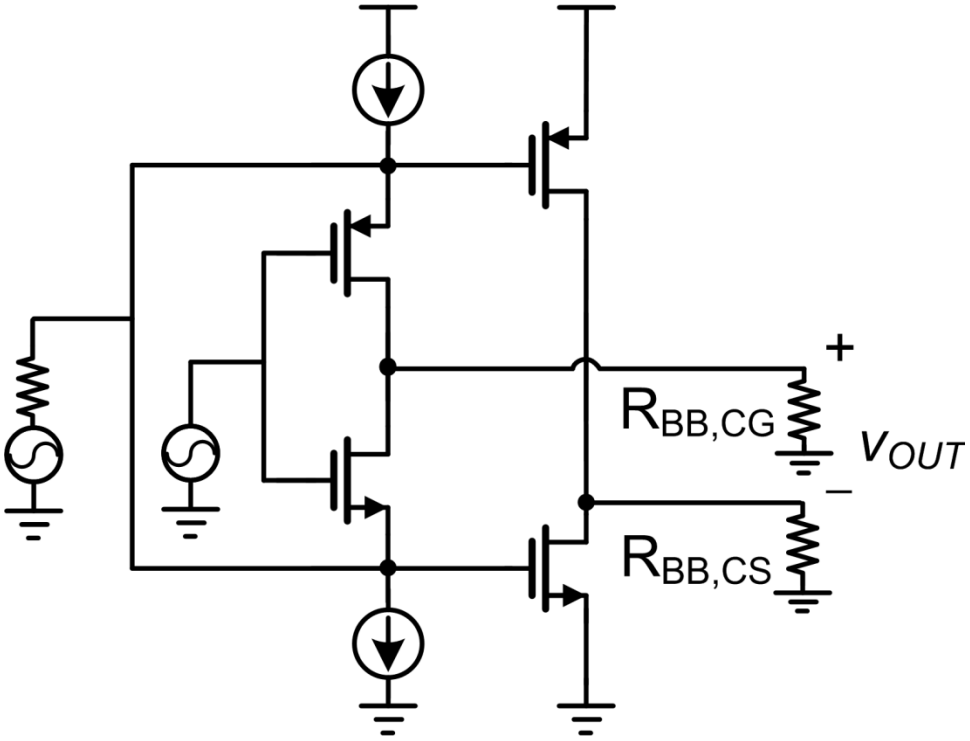
Noise cancellation condition

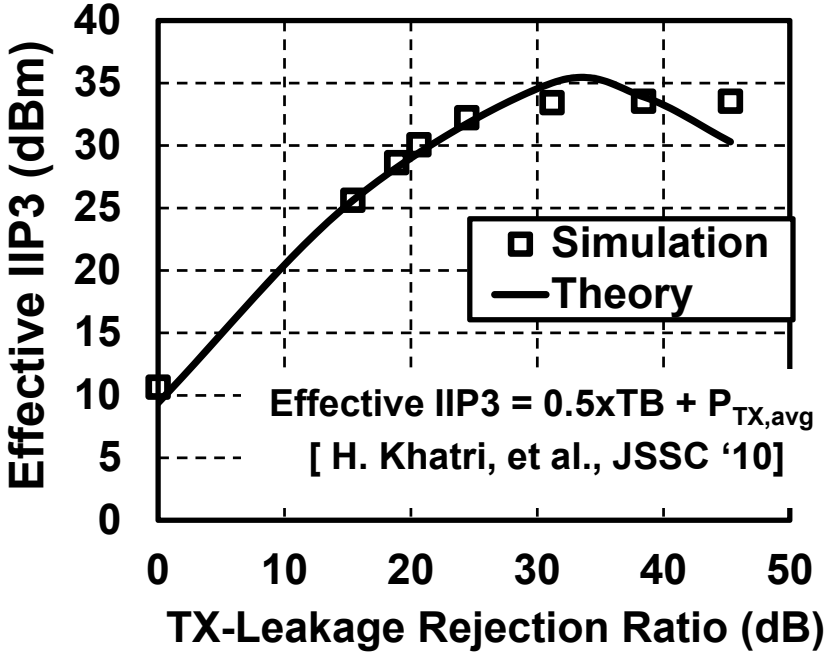
TX leakage cancellation (α_{1T}~0)

$$TB^{-1} \equiv \frac{\text{Cross-mod. Dist.}}{\text{In-band Jammer}} \propto \left(g_{m2}R_S - \frac{R_{BB,CG}}{R_{BB,CS}} \right) \alpha_{3T^2S} + \left[g'_{m2}\left(\alpha_{2T} + \alpha_{2TS}\alpha_{1T} \right) + \frac{1}{2} g''_{m2} \alpha^2_{1T} \right] \frac{R_S}{2}$$

$$\boxed{TB^{-1} \propto \alpha_{2T} g'_{m2} R_S}$$

Effective IIP3 with Leakage Cancellation

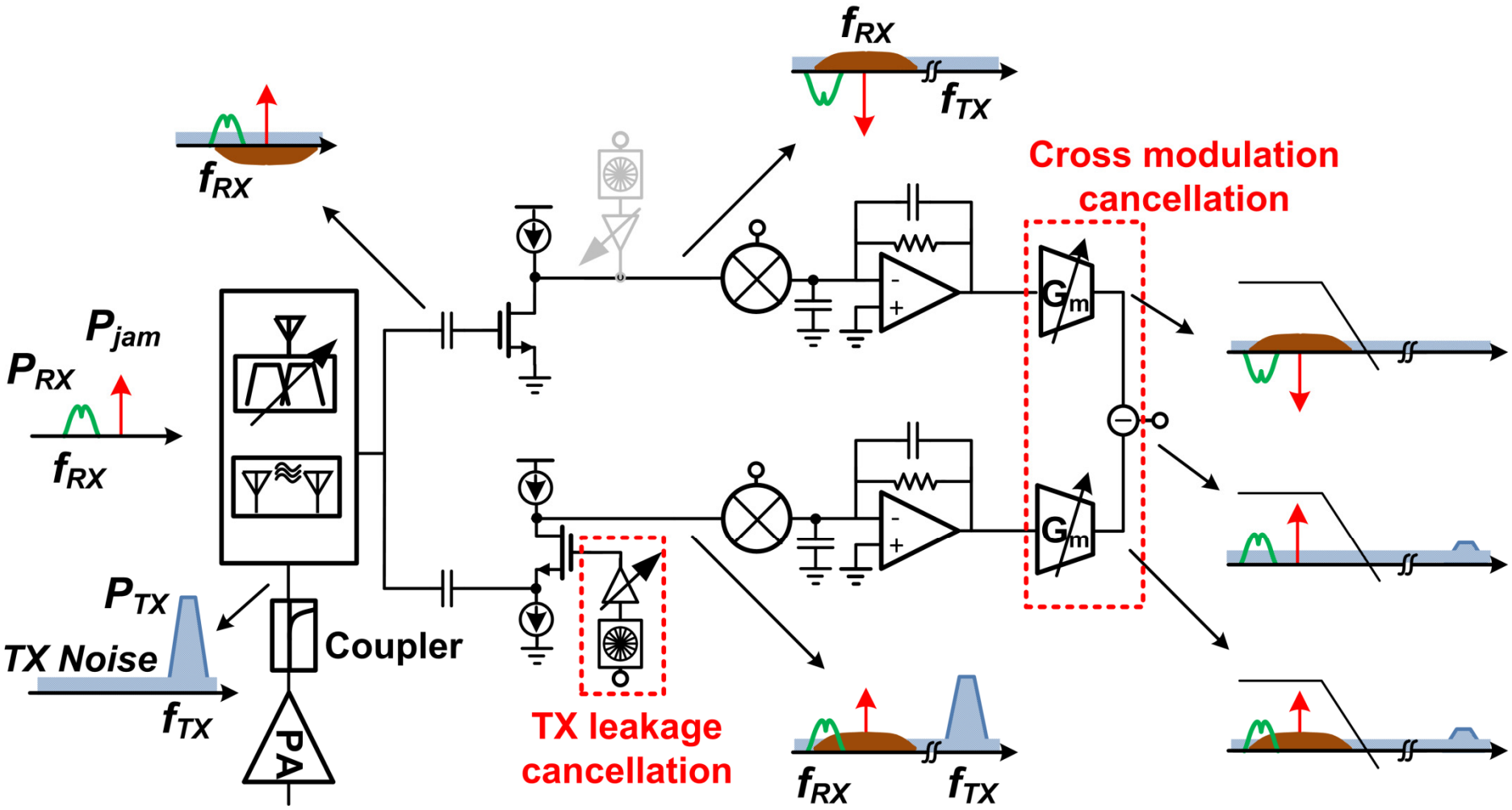




$$TB^{-1} \equiv \frac{\text{Cross-mod. Dist.}}{\text{In-band Jammer}} \propto \left(g_{m2}R_S - \frac{R_{BB,CG}}{R_{BB,CS}} \right) \alpha_{3T^2S} + \left[g'_{m2}\left(\alpha_{2T} + \alpha_{2TS}\alpha_{1T} \right) + \frac{1}{2} g''_{m2} \alpha^2_{1T} \right] \frac{R_S}{2}$$

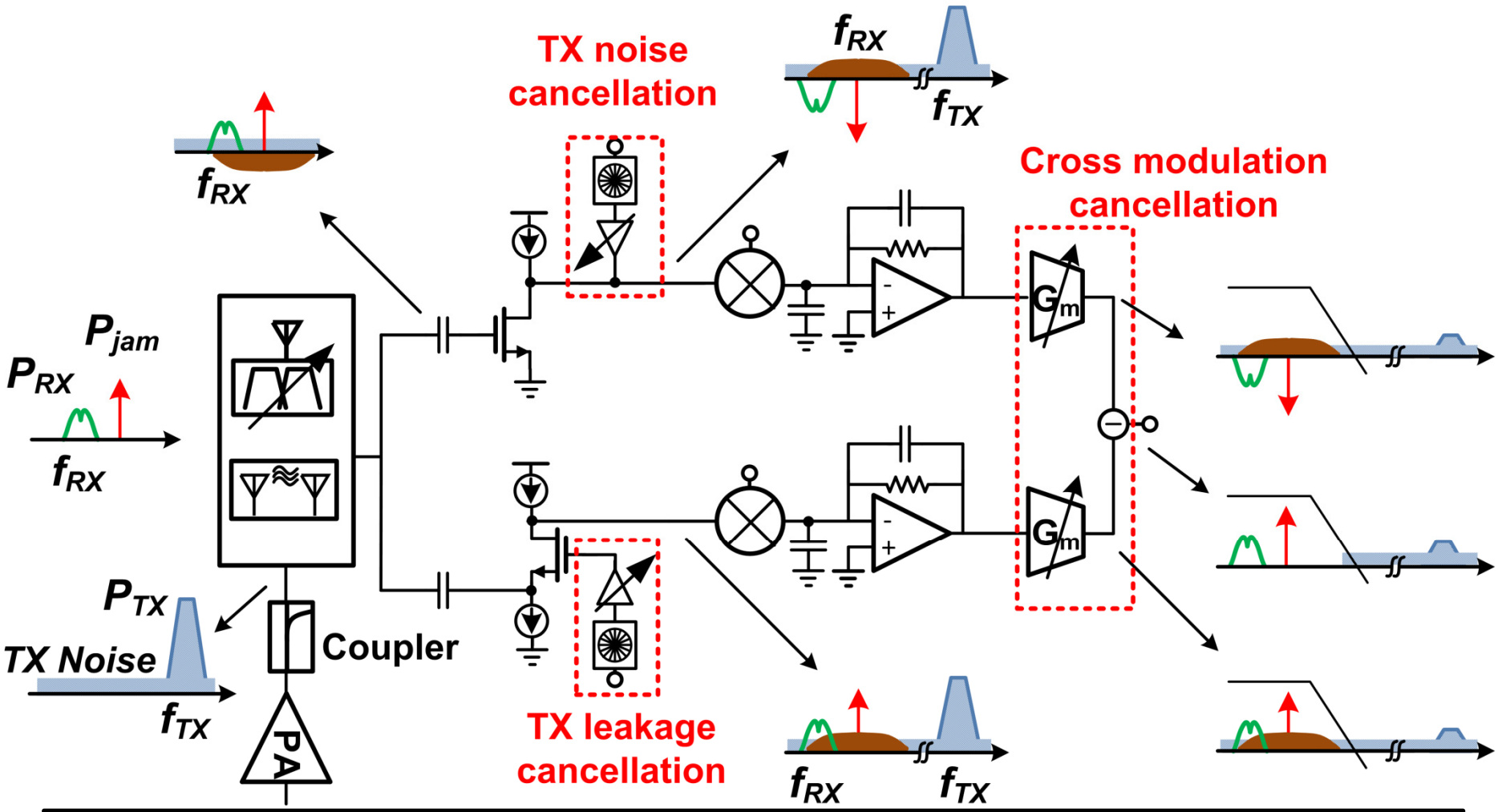
A highly-linear complementary LNTA enables low residual cross modulation (high effective OOB IIP3).

TX Noise in the RX Band



TX noise in the RX band is still an issue.

Cancellation of TX Noise in RX Band

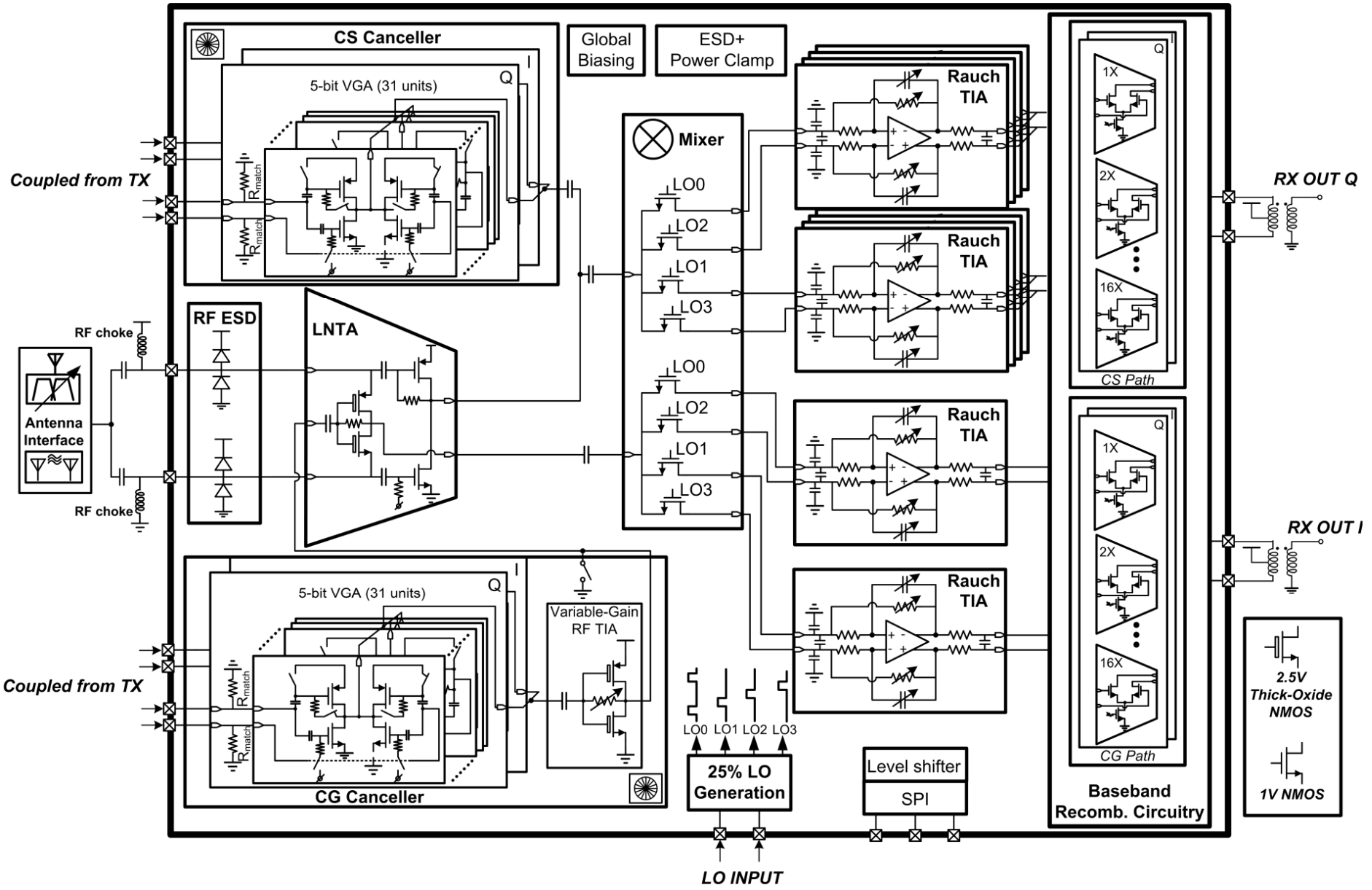


With appropriate scaling in the 2nd injection path, TX noise in the RX band is cancelled upon recombination.

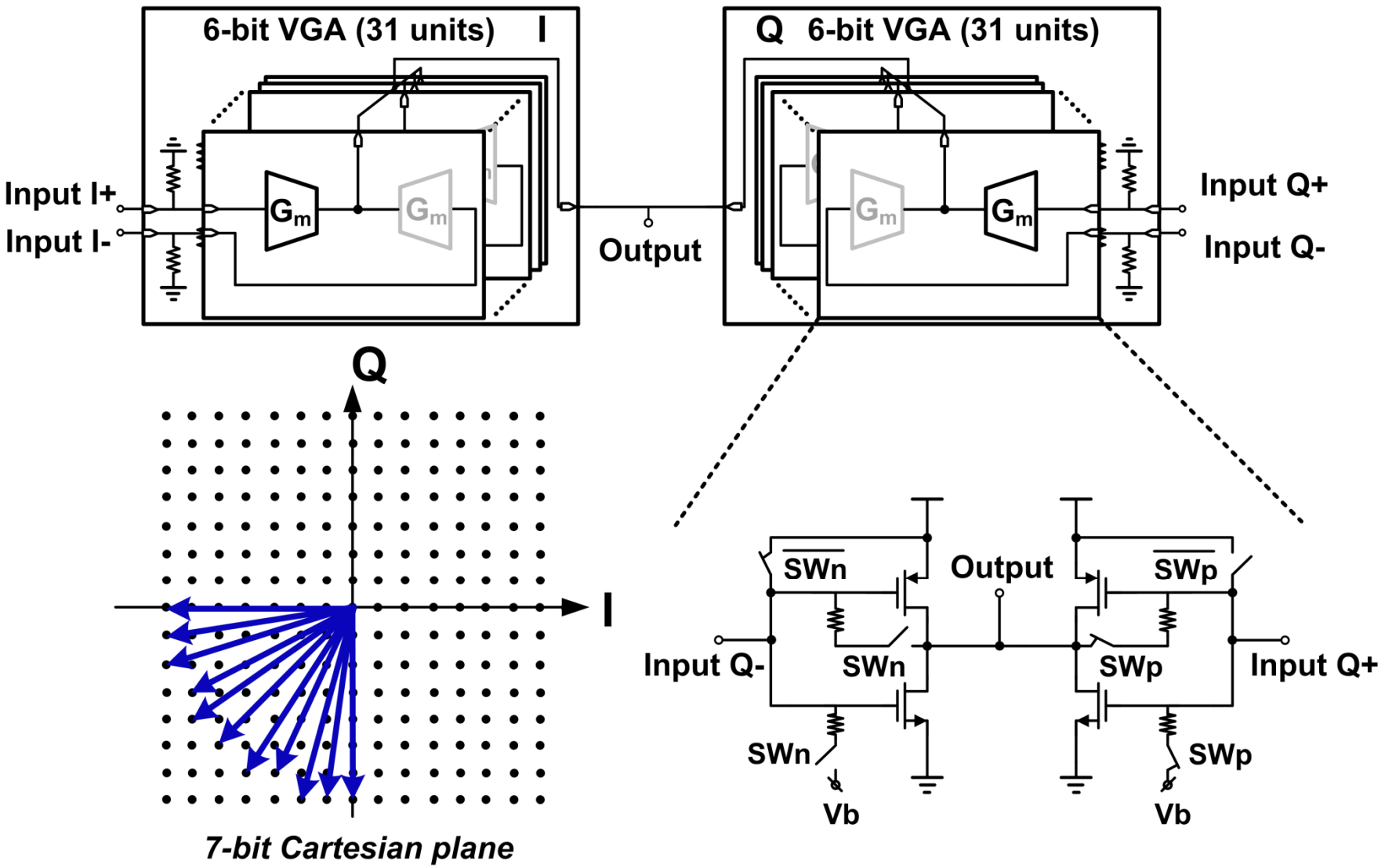
Presentation Outline

- Introduction
- Low-Noise Active Cancellation of TX Leakage and TX Noise in RX-Band
- A 65nm CMOS Implementation
- Measurement Results

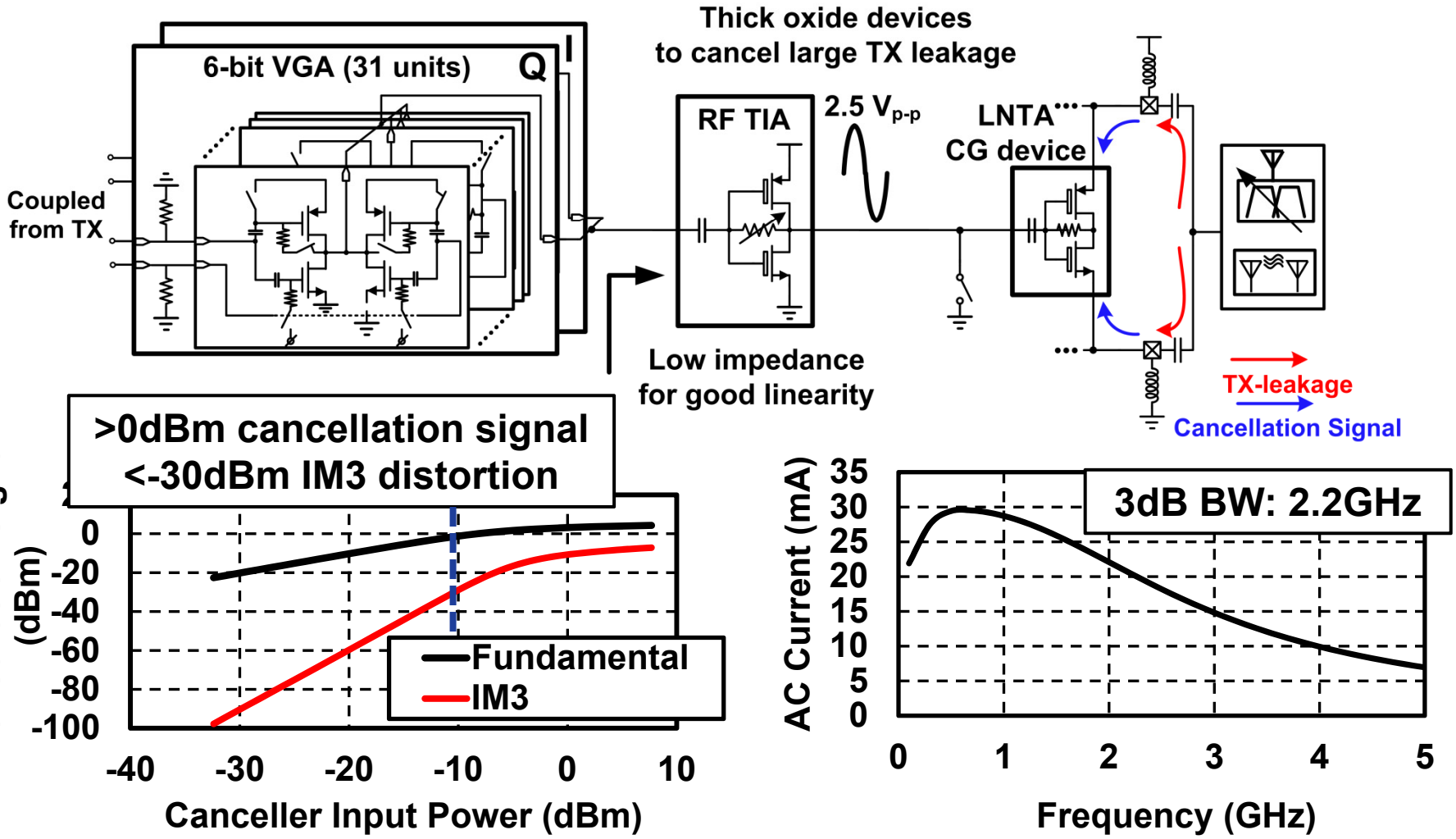
Block Diagram and Schematic



Cartesian Phase Rotator



CG-Path TX-Leakage Canceller



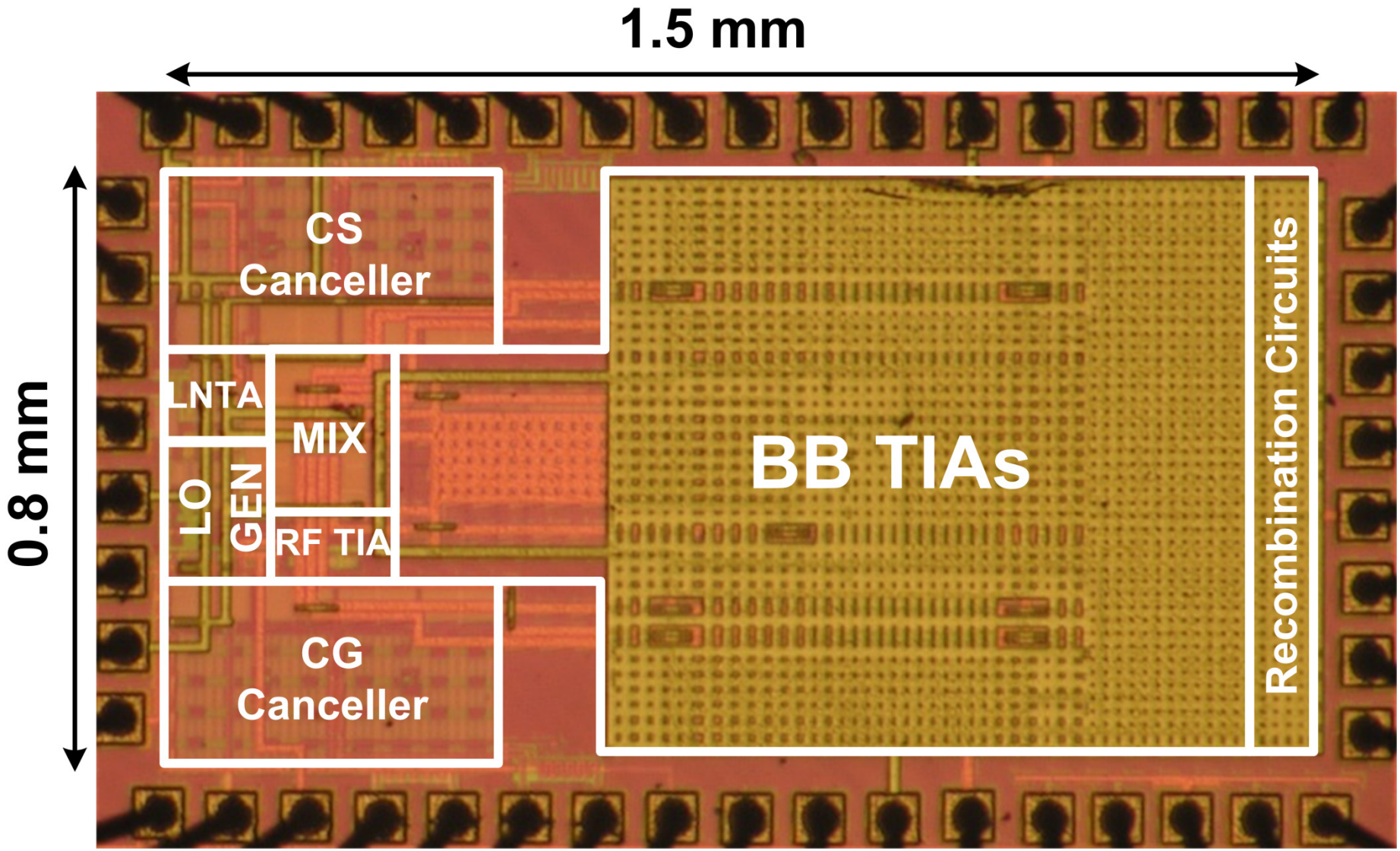
Thick-oxide devices are used in the cancellation path for cancellation of >0dBm peak TX leakage.

Other Circuits

- Passive Mixer
  - 4-phase mixing is used here for simplicity.
  - 8-phase mixing would lower the NF further by reducing the noise folding effect.
- Baseband Rauch TIA
  - Second order filtering for high selectivity and low in-band input impedance*.
  - Large input shunt capacitors to help sink out-of-band TX-leakage.
- Recombination Circuits
  - 5-bit binary-weighted Gm cells for programmable complex recombination weights.

* I. Fabiano, et al., “SAW-less analog front-end receivers for TDD and FDD”, ISSCC 2013

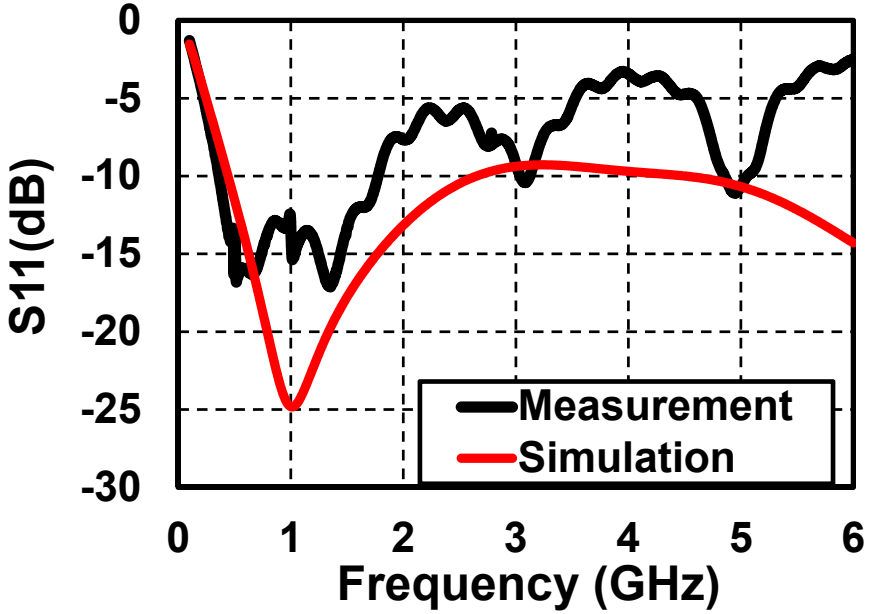
65nm CMOS Receiver Prototype

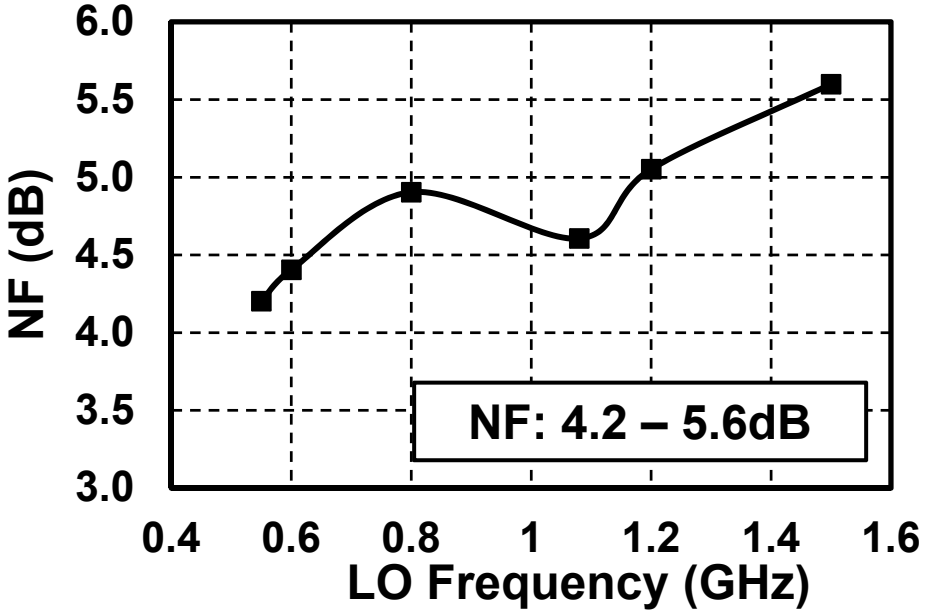


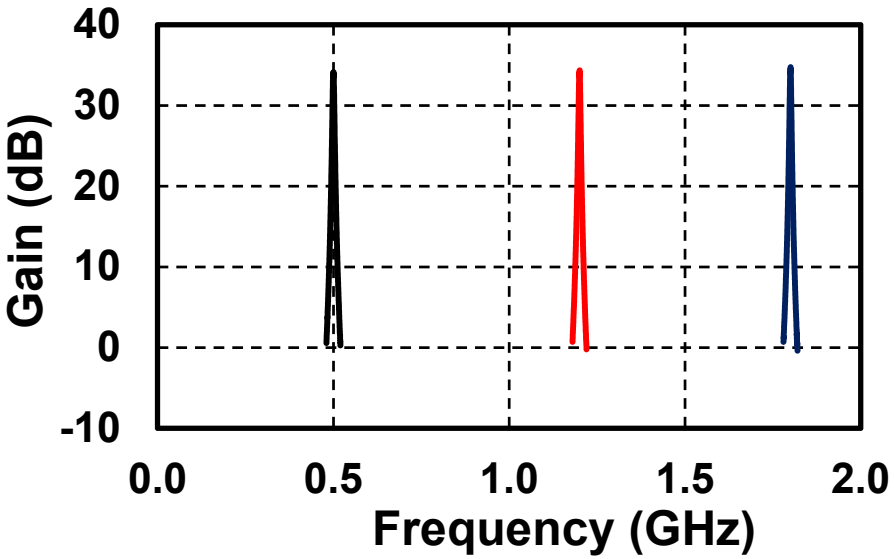
Presentation Outline

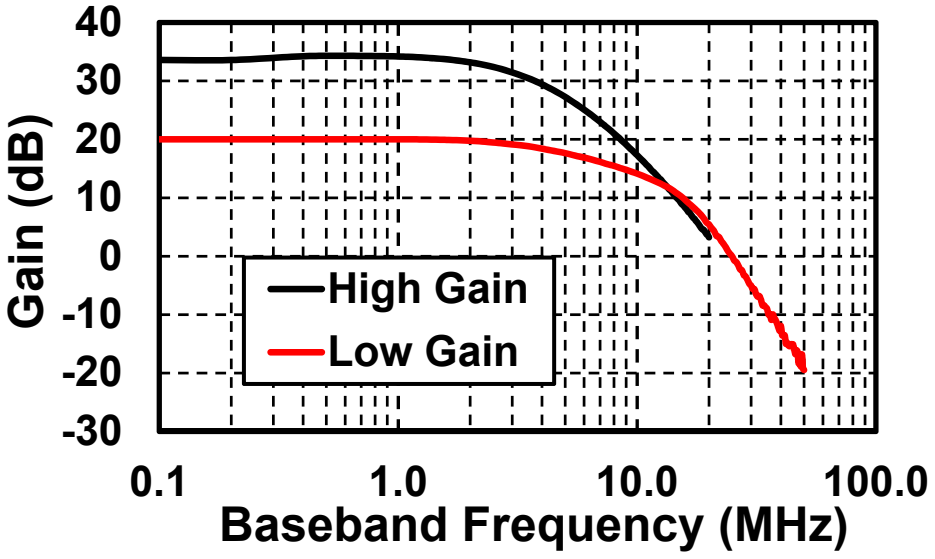
- Introduction
- Low-Noise Active Cancellation of TX Leakage and TX Noise in RX-Band
- A 65nm CMOS Implementation
- Measurement Results

Receiver Measurement Results

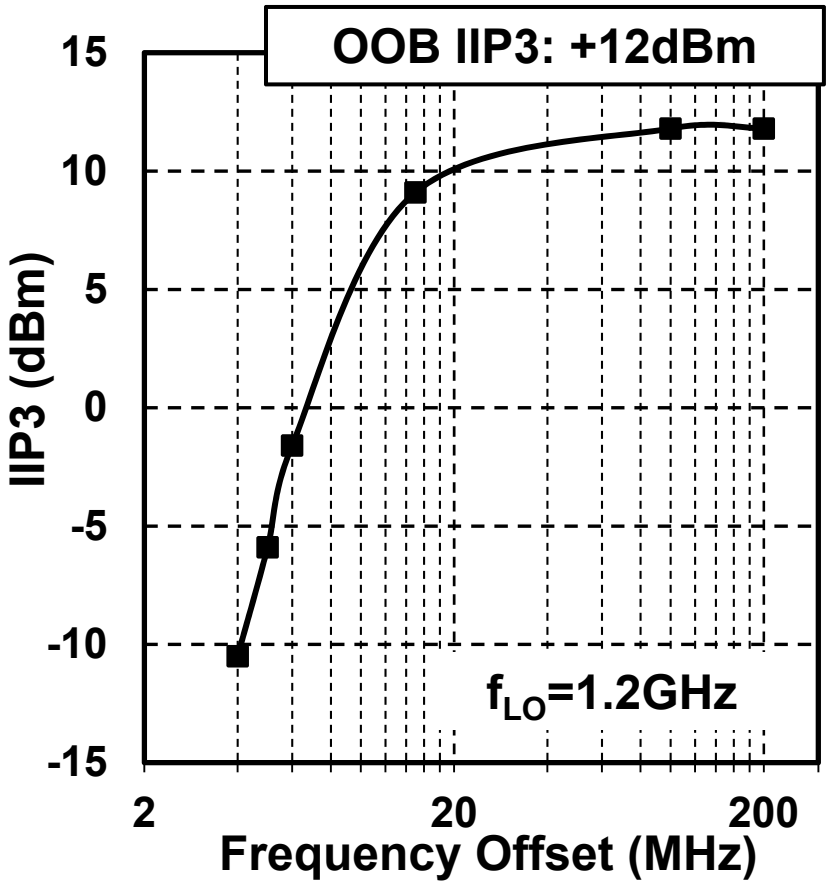


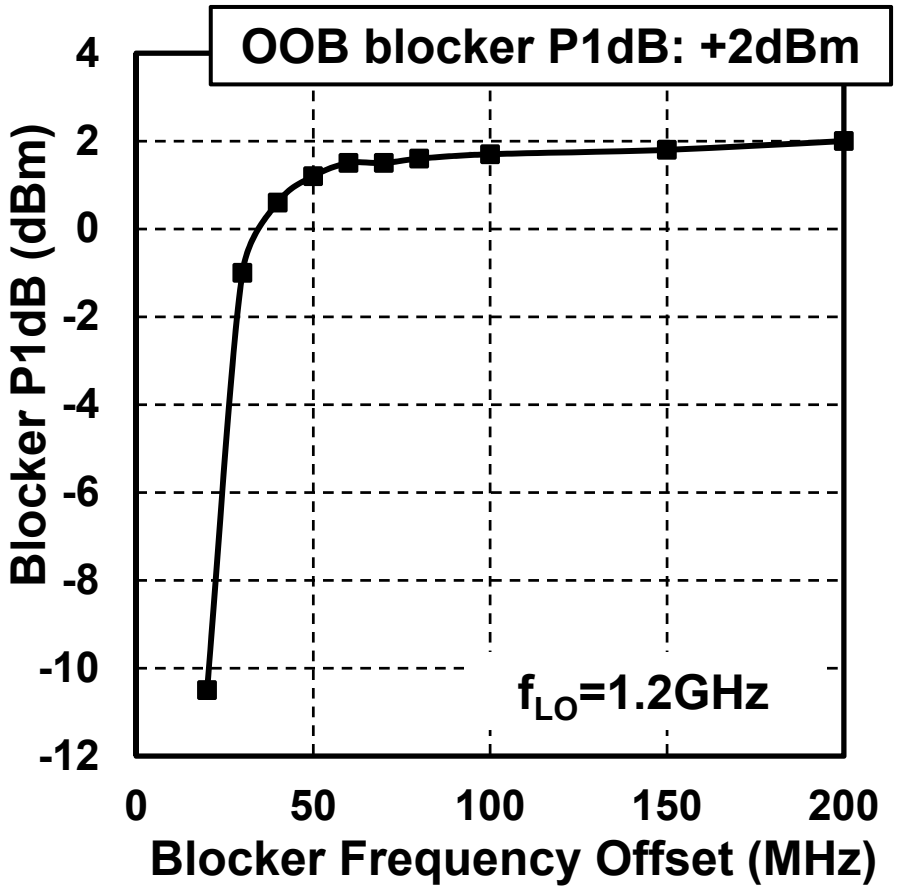






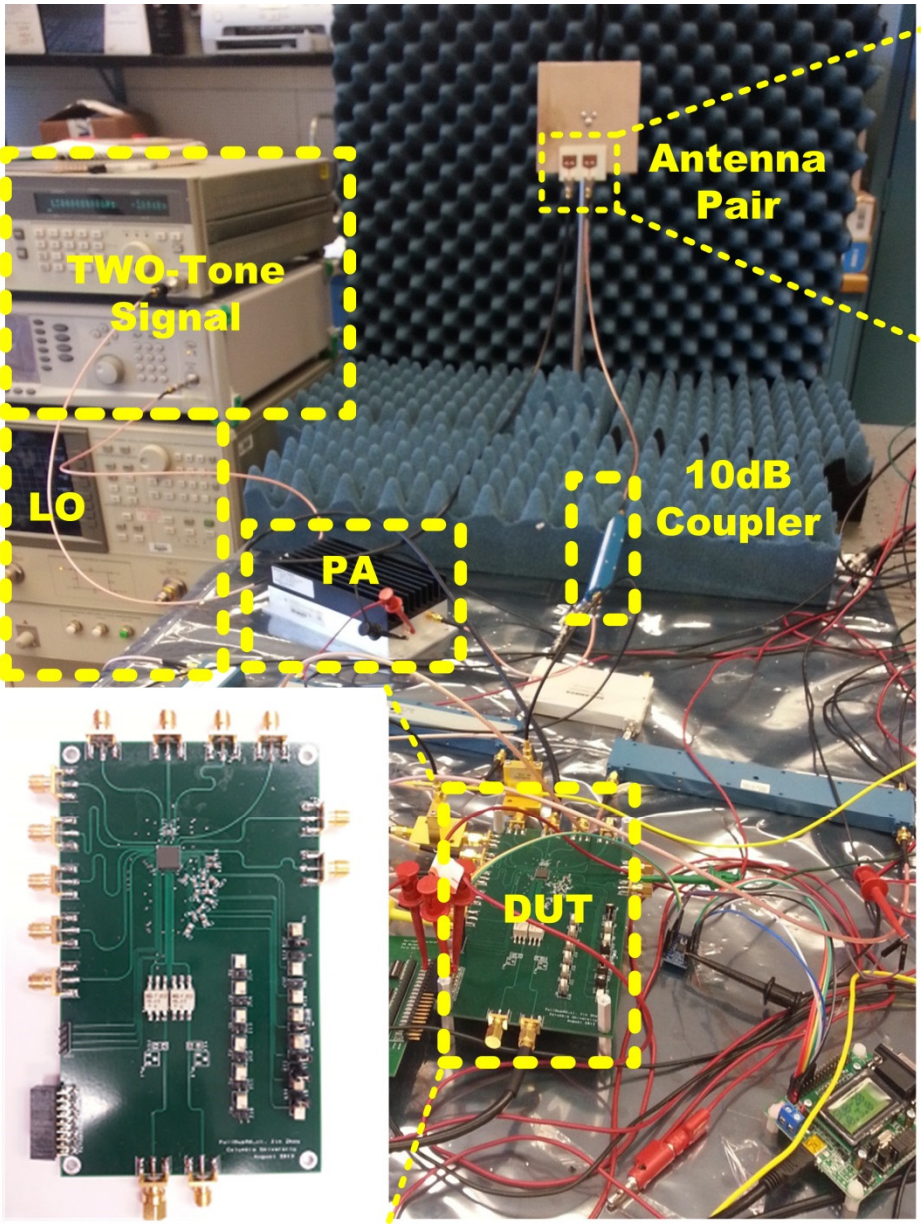
Linearity Measurements

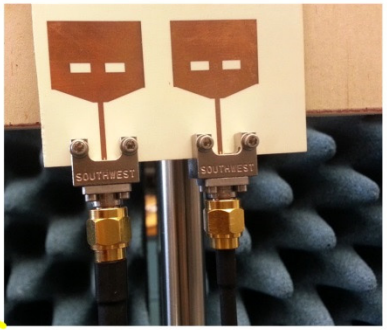


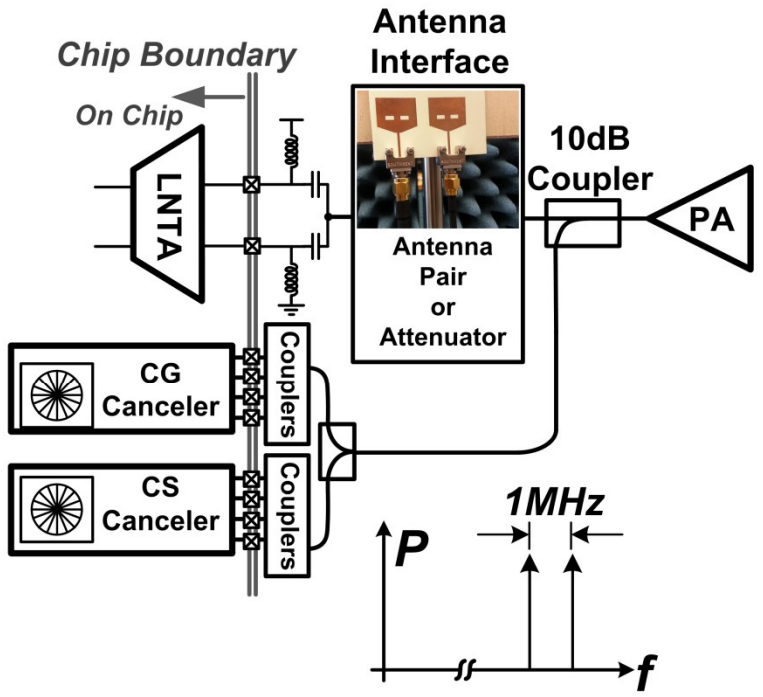


- Out-of-band linearity that is typical of current-mode design is achieved.
- This linearity, however, is still insufficient to handle >0dBm TX leakage without cancellation.

Leakage Cancellation Setup

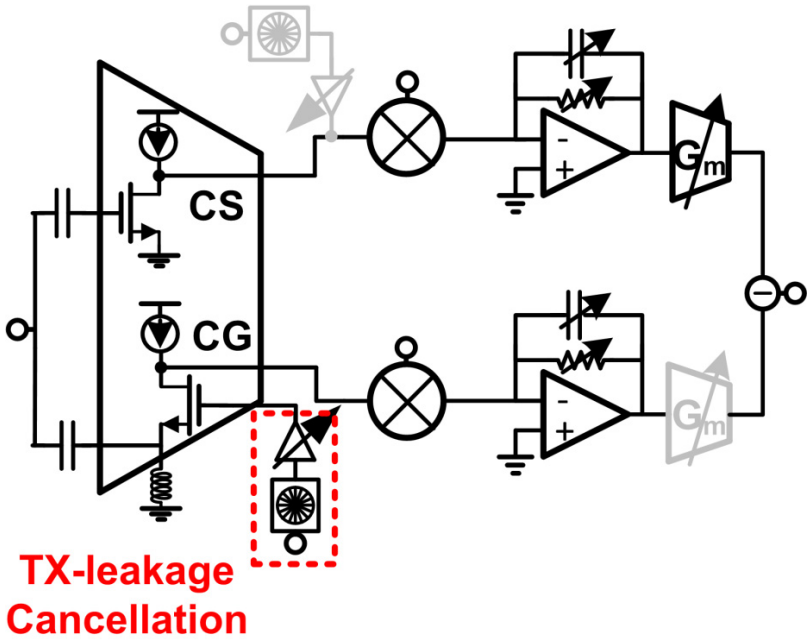


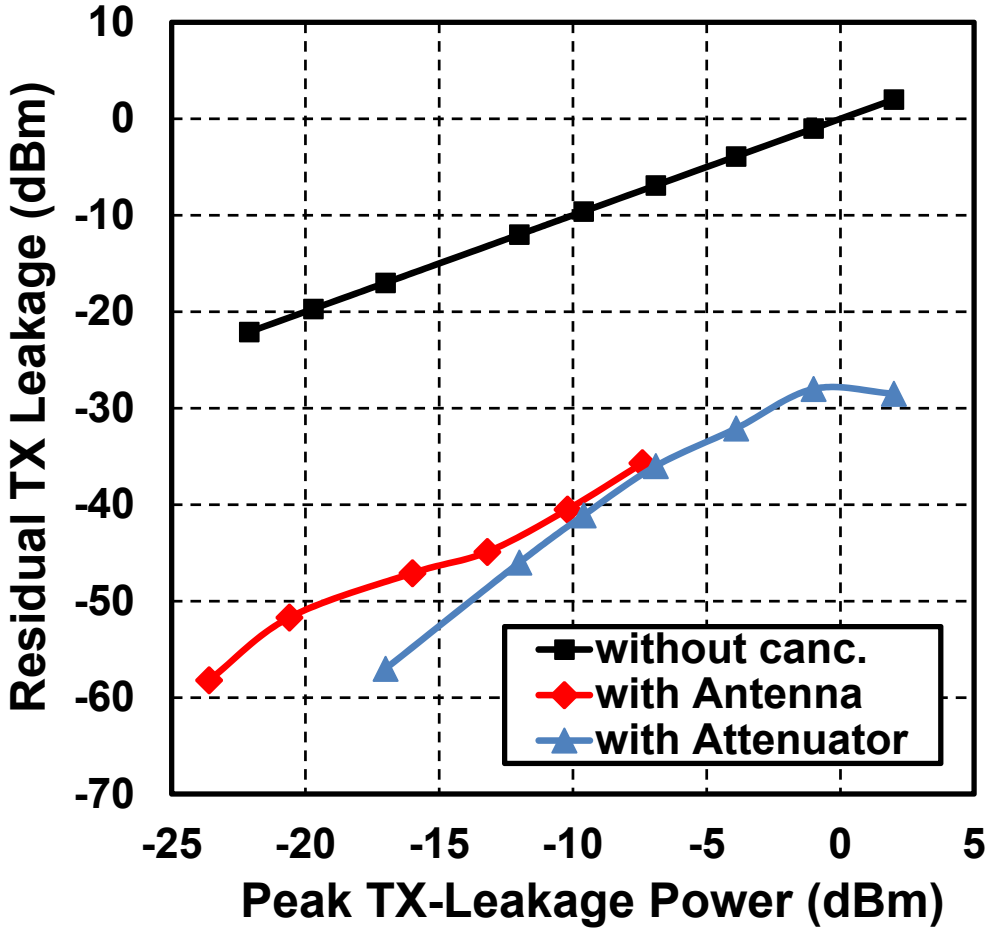




f_{RX}=1.2GHz f_{TX}=1.305GHz

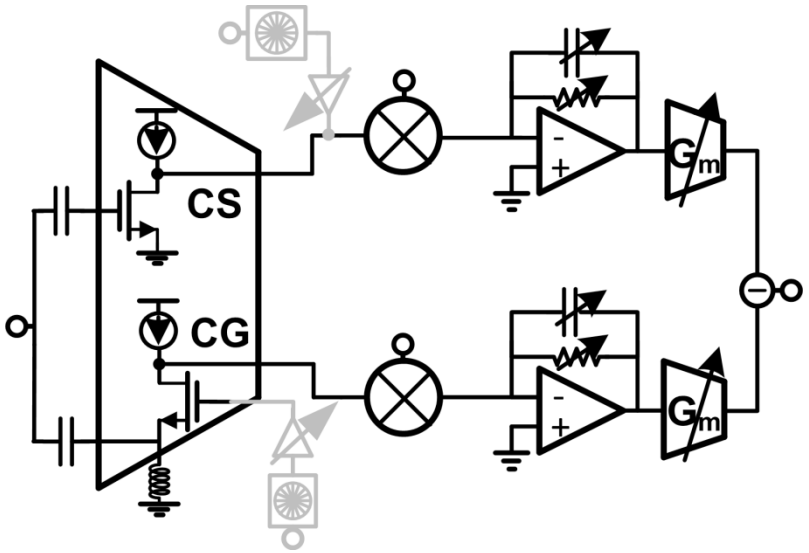
TX-Leakage Cancellation Measurements





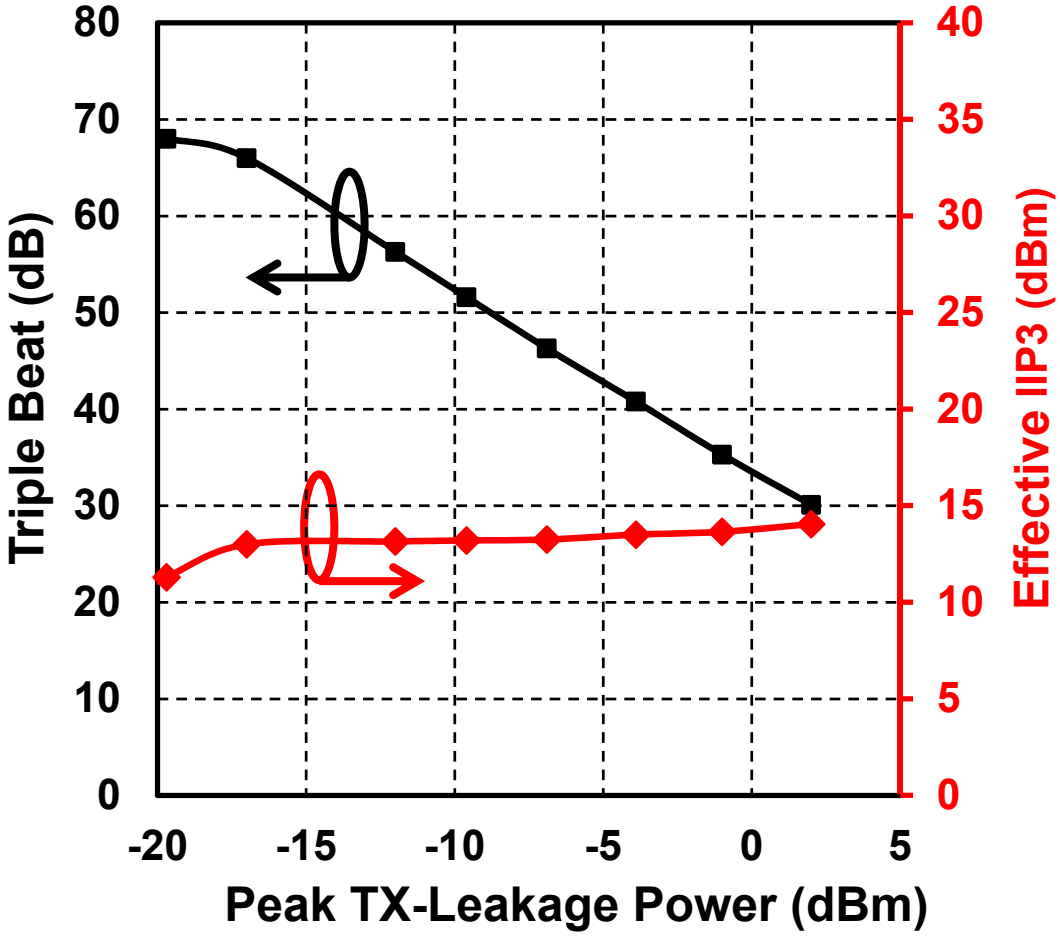
TX leakage canceller is able to cancel up to +2dBm peak TX leakage with 30dB suppression.

TB Measurements without Cancellation



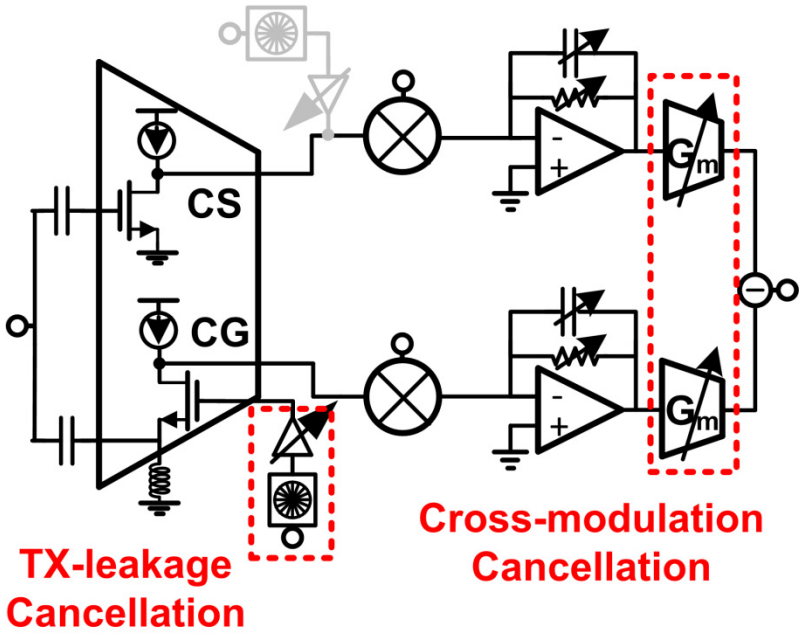
Effective IIP3 = 0.5xTB + $P_{TX,avg}$

[H. Khatri, et al., JSSC, 2010]



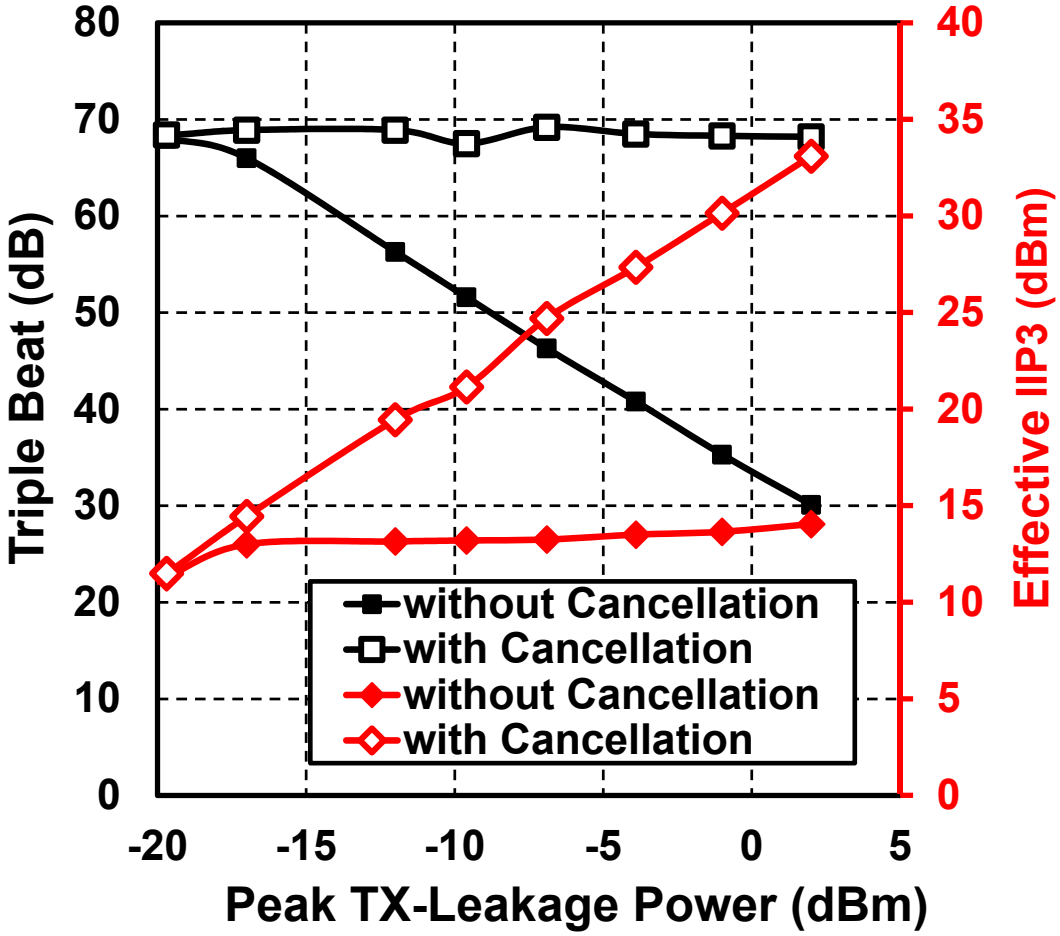
For the RX without cancellation, TB decreases at 20dB/decade as TX leakage power increases.

TB Measurements with Cancellation



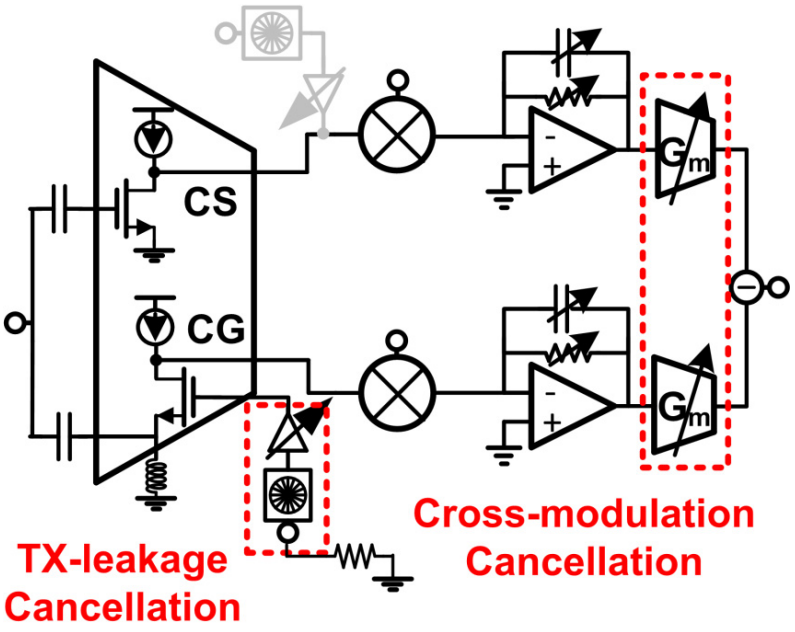
Effective IIP3 = 0.5xTB + $P_{TX,avg}$

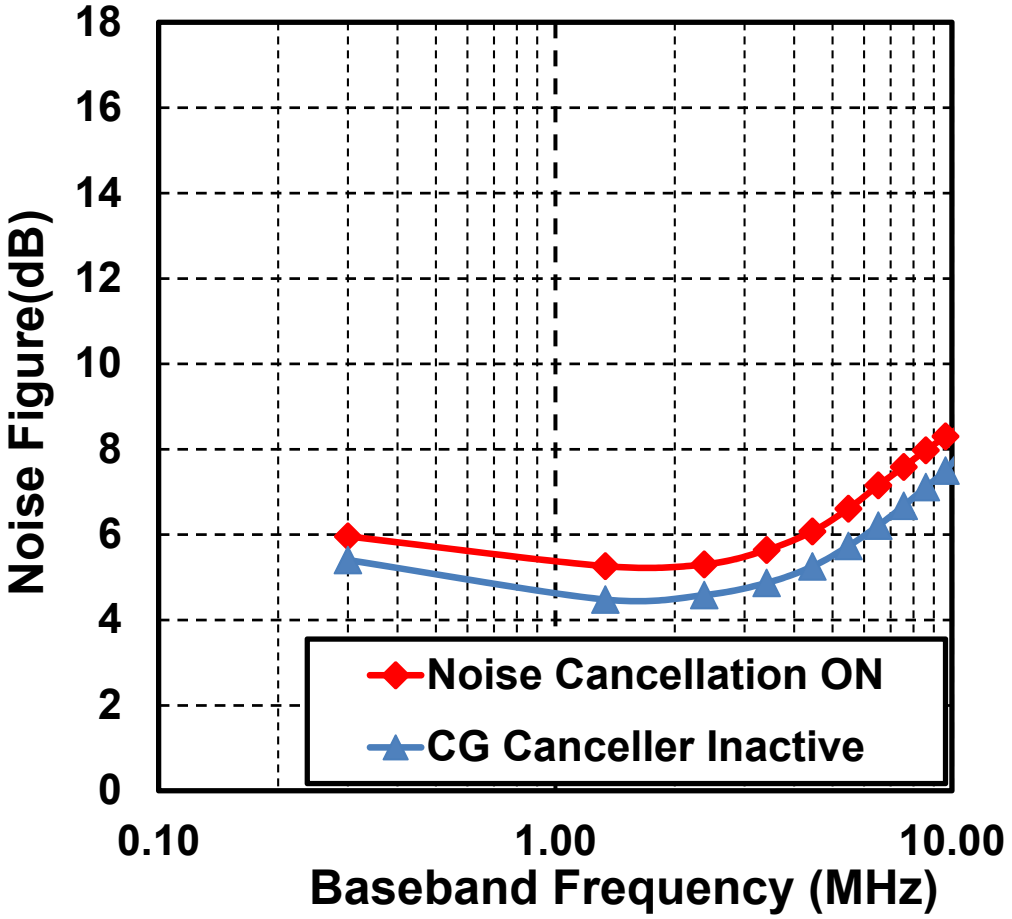
[H. Khatri, et al., JSSC, 2010]



TB_{2dBm} of 68dB and an effective IIP3 of +33dBm (enhancements of 38dB and 19dB, respectively).

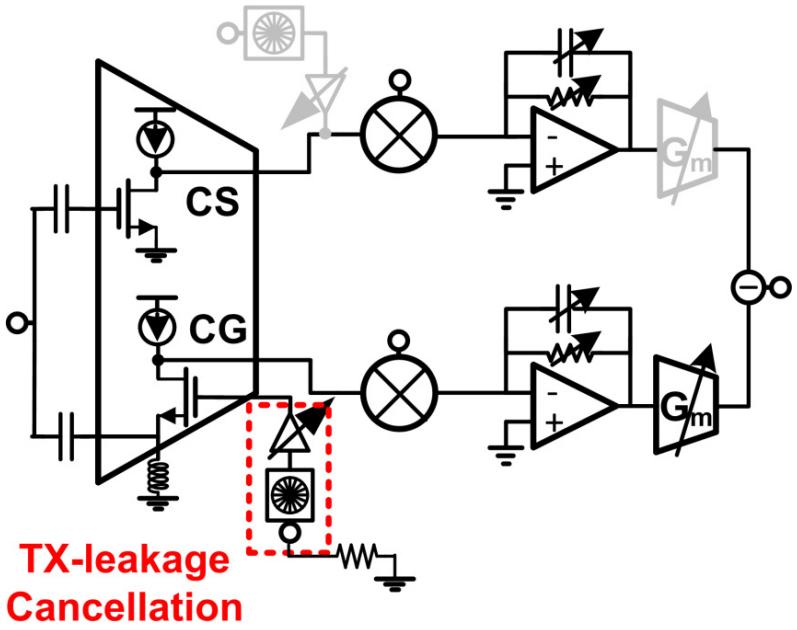
Receiver NF with CG-Canceller Active

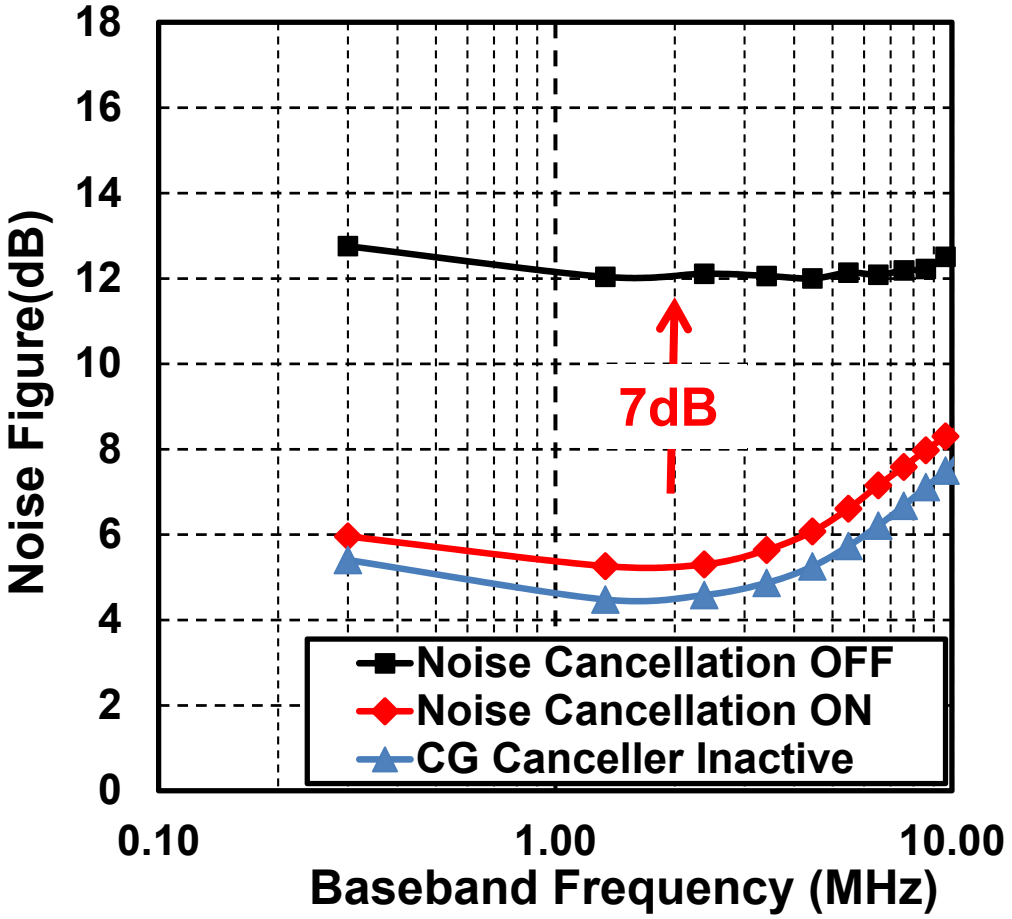




NF degradation due to CG canceller and setting of recombination for cross-mod. cancellation is <0.8dB.

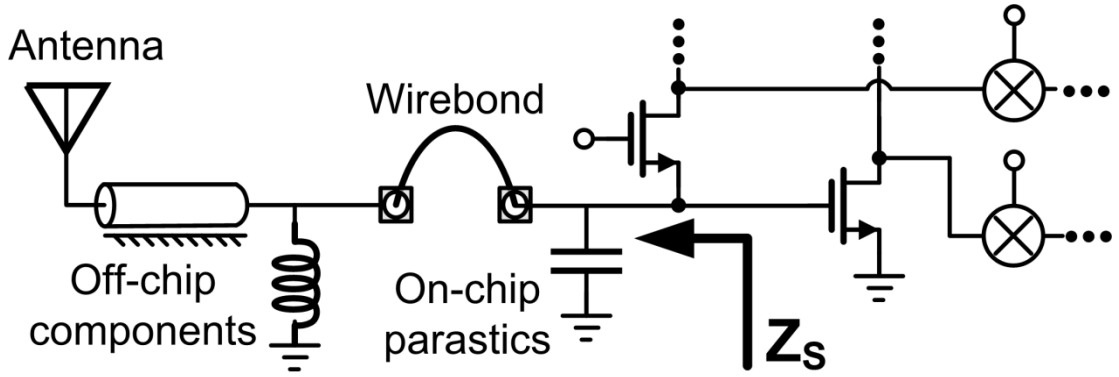
Receiver NF with CG-Canceller Active

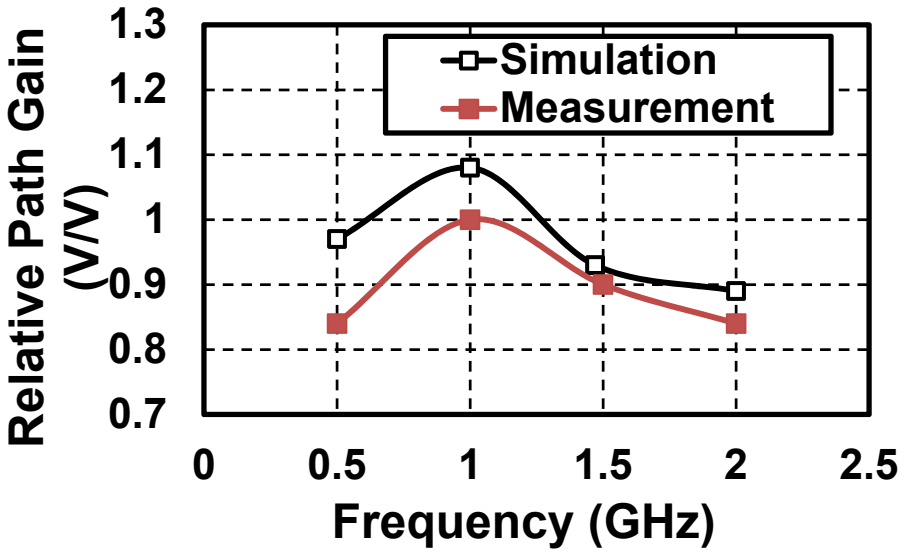


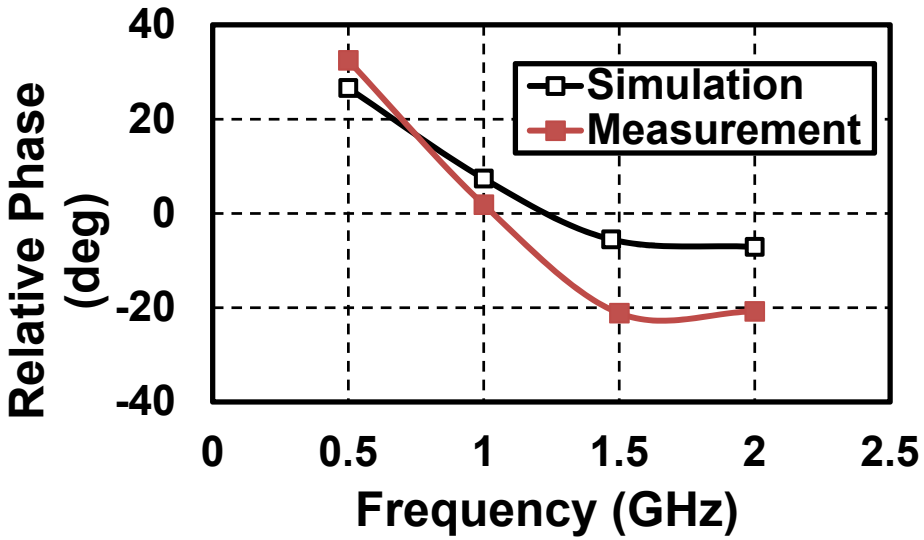


Without noise cancellation, 7dB NF degradation is measured.

Optimum NF Condition with Varying Z_S

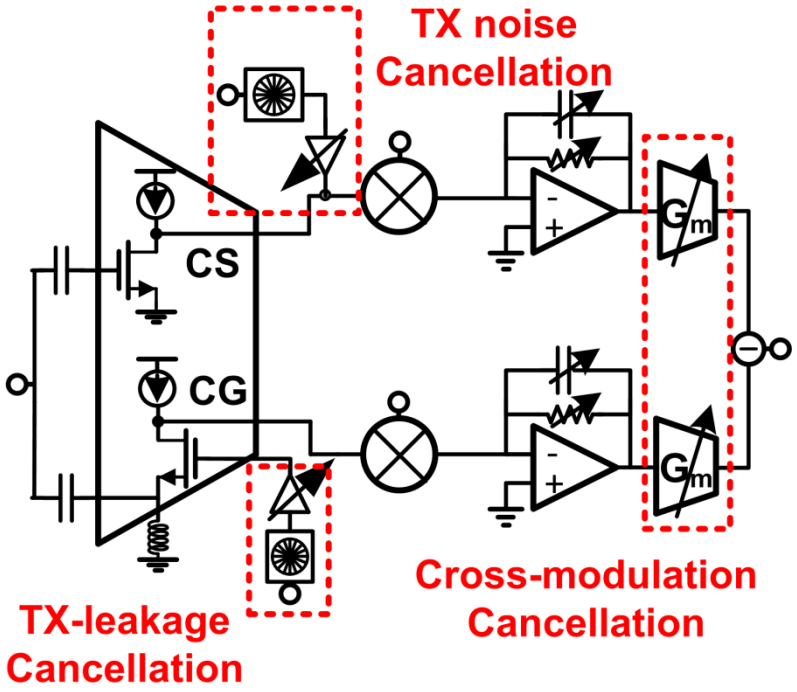


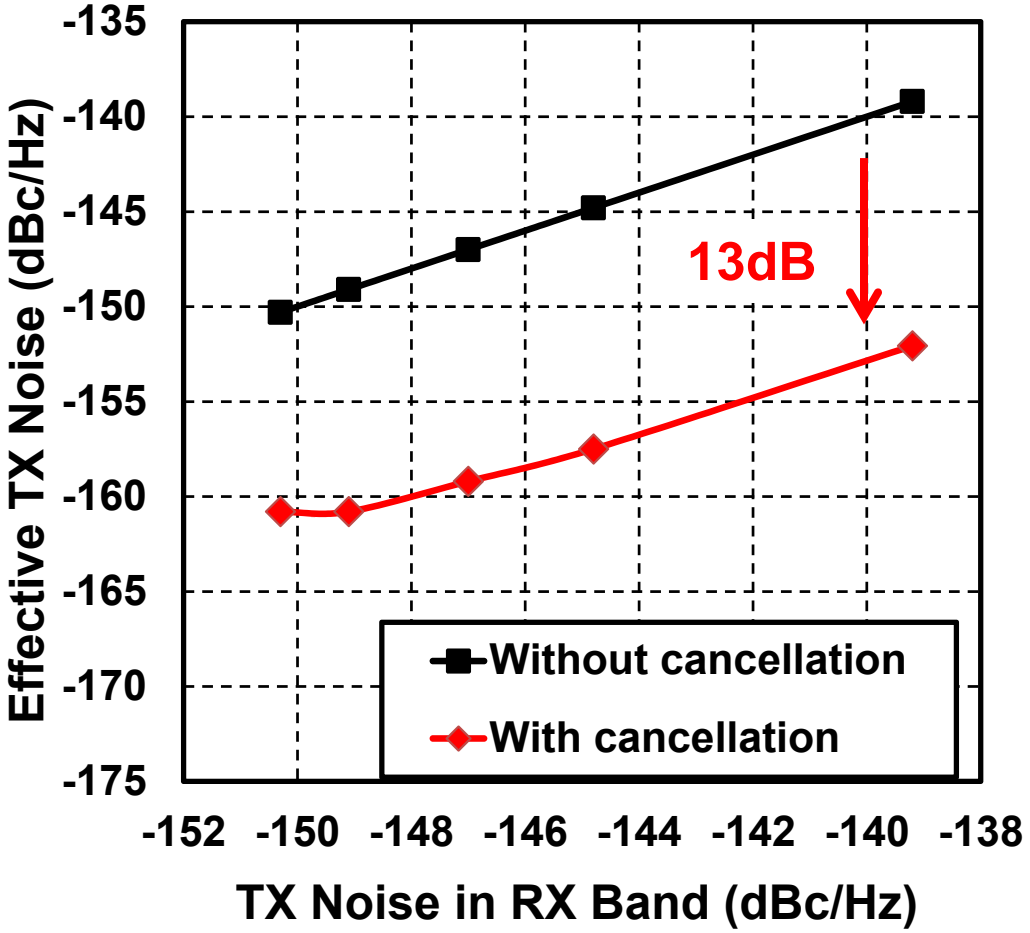




Optimum noise condition closely matches simulations.

TX Noise Cancellation Measurements





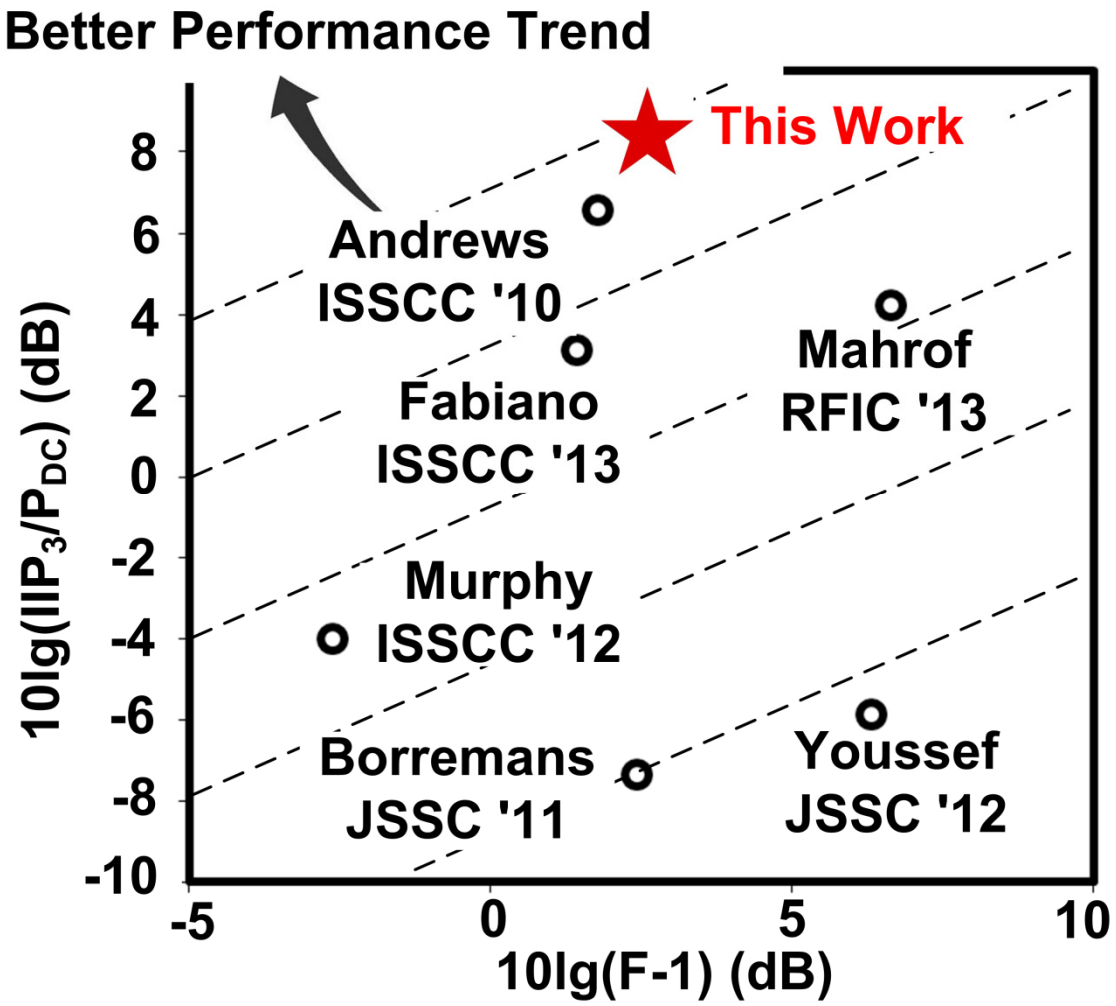
CS canceller improves the effective TX noise by up to 13dB.

Performance Summary and Comparison

Work	Khatri '10	Andrews '10	Fabiano '13	**This work**
Architecture	TX Leakage Suppression	Highly-Linear Software-Defined Receiver		**Active Multi-point TX Leakage Cancellation**
RF Frequency (GHz)	1.96	0.1-2.4	1.8-2.1	**0.3-1.7**
Baseband BW (MHz)	N/A	1.6	1.4/3.2	**2-76**
DSB NF (dB)	3.1	4	3.1	**4.2**
OOB IIP3 (dBm)	N/A	+25	+16	**+12/+33[1]**
NF Degradation due to Leakage Cancellation (dB)	1.8	N/A	N/A	**<0.8**
TB @ 2dBm peak TX Leakage (dB)	9[2]	52[3]	34[3]	**30 (w/o cancellation) 68 (with cancellation)**
TX Noise Cancellation	Not Implemented	Not Implemented	Not Implemented	**13dB**
RX Power Consumption (mW)	114	37-70	31	**75-83**
Canceller Power Consumption (mW)	48	N/A	N/A	**13-72**
Area (mm^2)	N/A	2	0.74	**1.2**

[1] Effective IIP3 under cancellation of +2dBm peak TX leakage
[2] Calculated from reported TB at -28dBm TX leakage level
[3] Calculated from reported IIP3 (IIP3=0.5×TB+$P_{TX,avg}$ [Khatri, et al., JSSC 2010])

Figure of Merit Comparison



$$FOM = \frac{IIP3}{P_{DC} \times (F-1)}$$

The best linearity-versus-noise trade-off under modulated TX leakage when normalized for P_{DC}.

Conclusion

- A low-noise active TX-leakage cancellation technique is proposed that embeds the TX-leakage cancellation in a noise-cancelling LNTA.
- A second-point injection is used for TX noise cancellation.
- Analyses related to key design considerations are presented.
- A 65nm CMOS implementation validates the claims.

Acknowledgements

- This work was supported by the DARPA RF-FPGA program.

- Our thanks to
  - Dr. William J. Chappell from DARPA;
  - Anandaroop Chakrabarti from CoSMIC lab for invaluable layout assistance;
  - Ritesh Bhat, Jeffrey Chuang, Linxiao Zhang, Tolga Dinc and Jahnavi Sharma from CoSMIC lab, and Jianxun Zhu from CISL for valuable discussions, support and assistance.

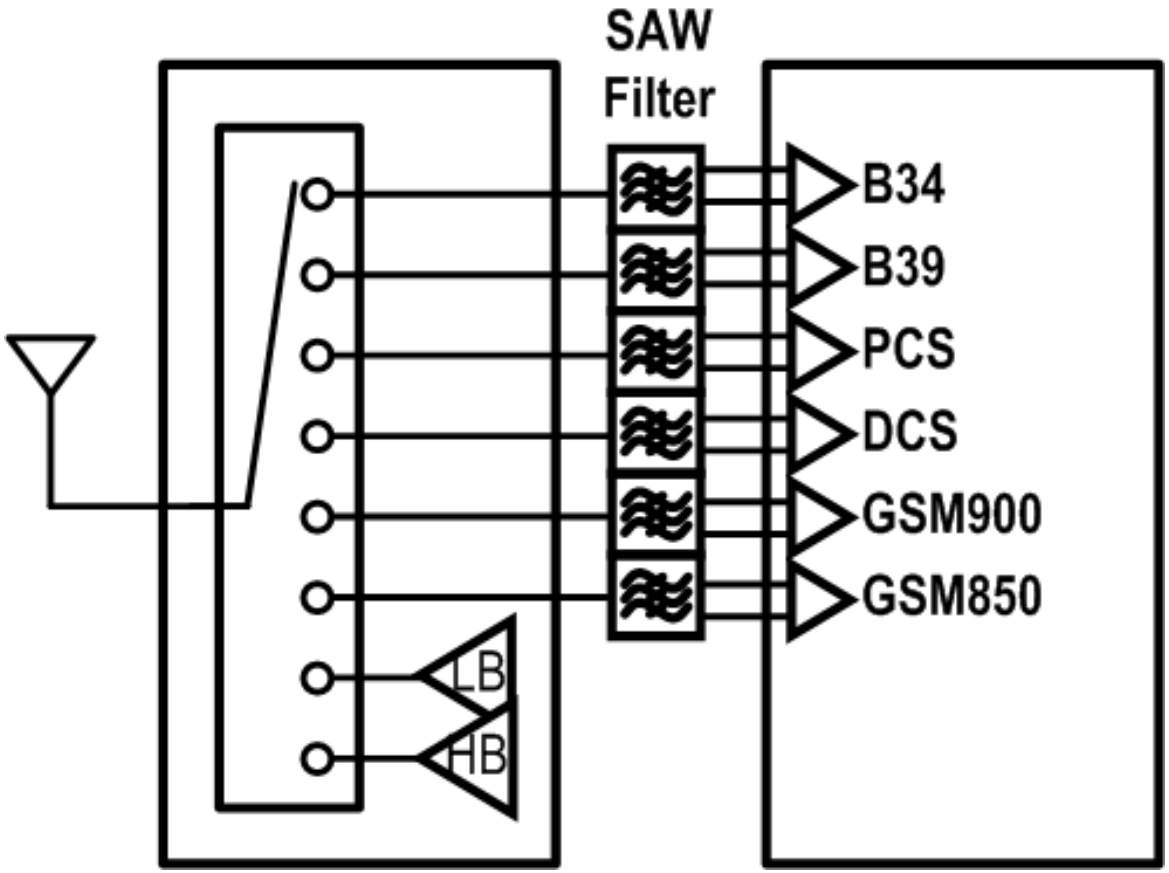
Thank you for your attention.

A Multi-Band Inductor-Less SAW-Less 2G/3G-TD-SCDMA Cellular Receiver in 40nm CMOS

Ming-Da Tsai, Chih-Fan Liao, Chi-Yun Wang, Yi-Bin Lee, Bosen Tzeng, Guang-Kaai Dehng

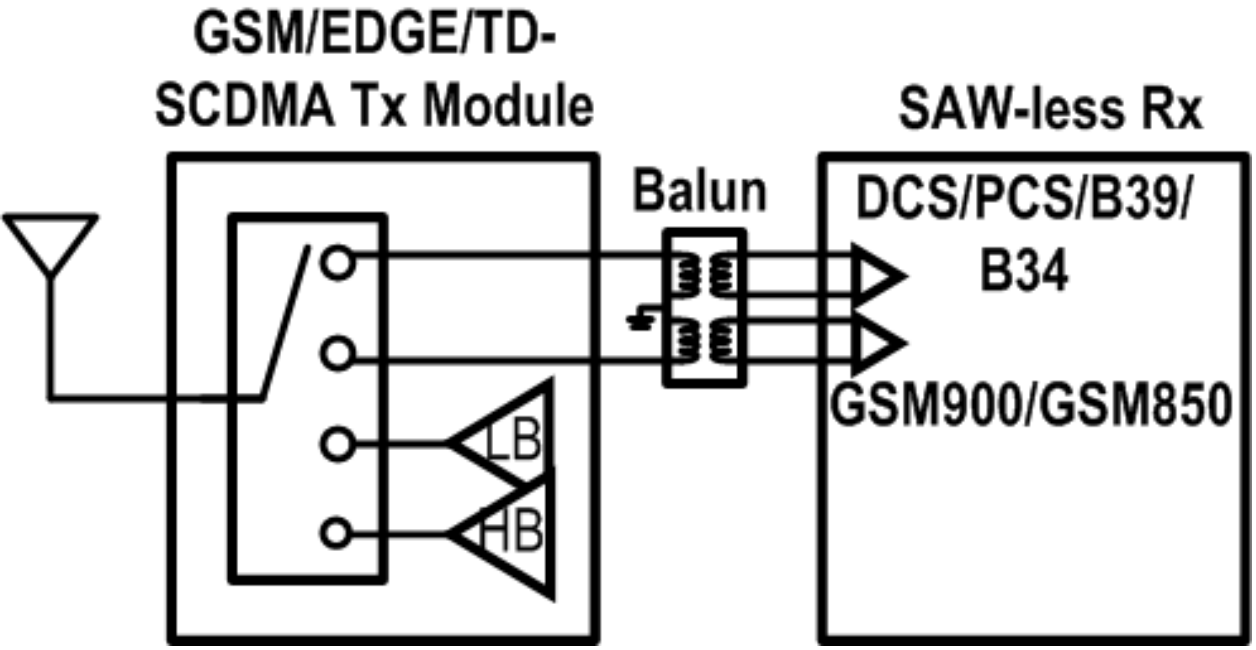
MediaTek, Hsinchu, Taiwan

Multi-band 2G/3G-TD-SCDMA RX



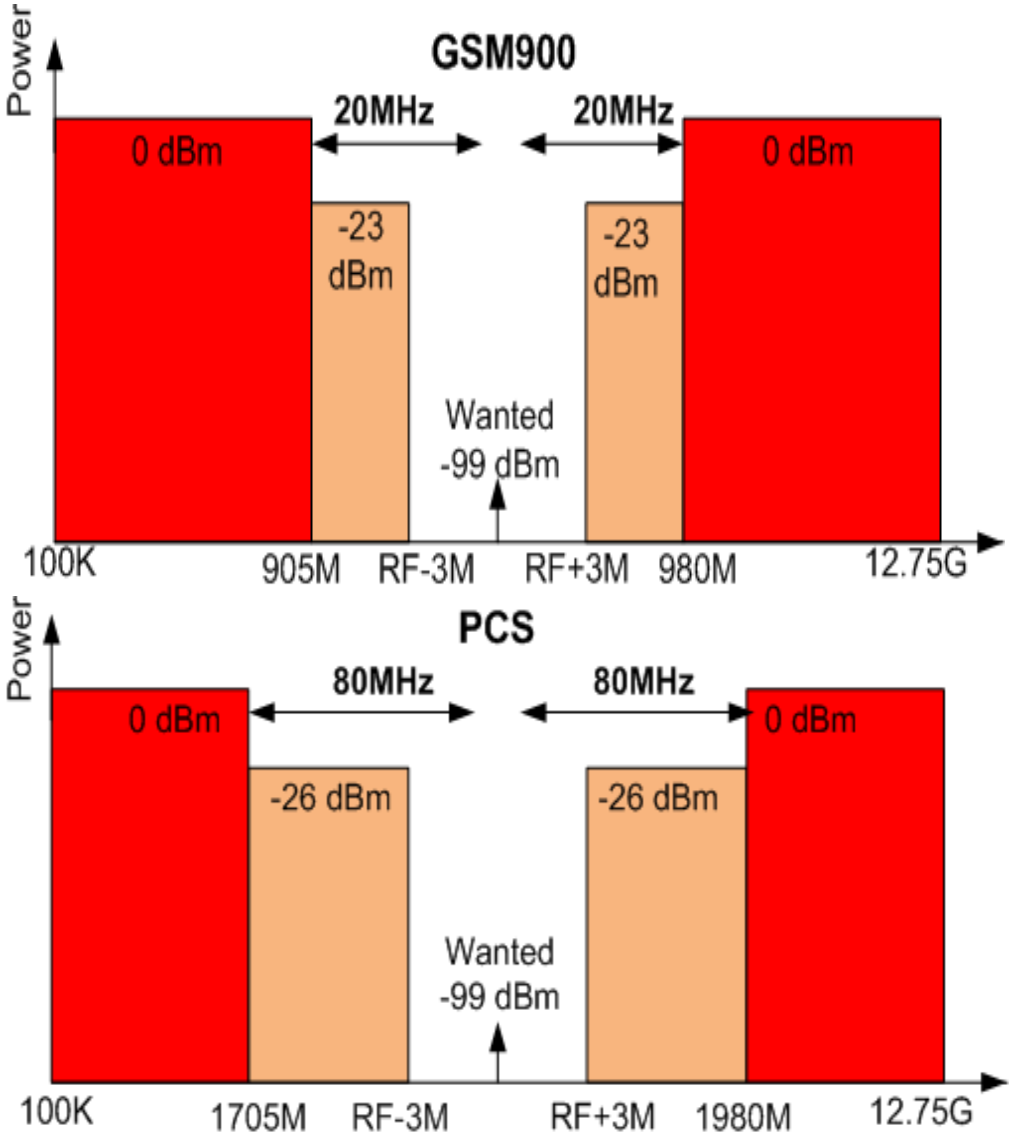
- 6 high Q SAW filters
- SAW protects the RX from OOB interferers

Multi-band SAW-less 2G/3G-TD-SCDMA RX



- OOB interferers go into the RX directly
- No SAW filter loss
- >50% lower eBOM cost
- Lower RX die cost

Multi-band SAW-less RX Challenges



- 0 dBm blocker at 20/80MHz offset from -99 dBm desired signal
- 1 Vpp at chip input with matching gain

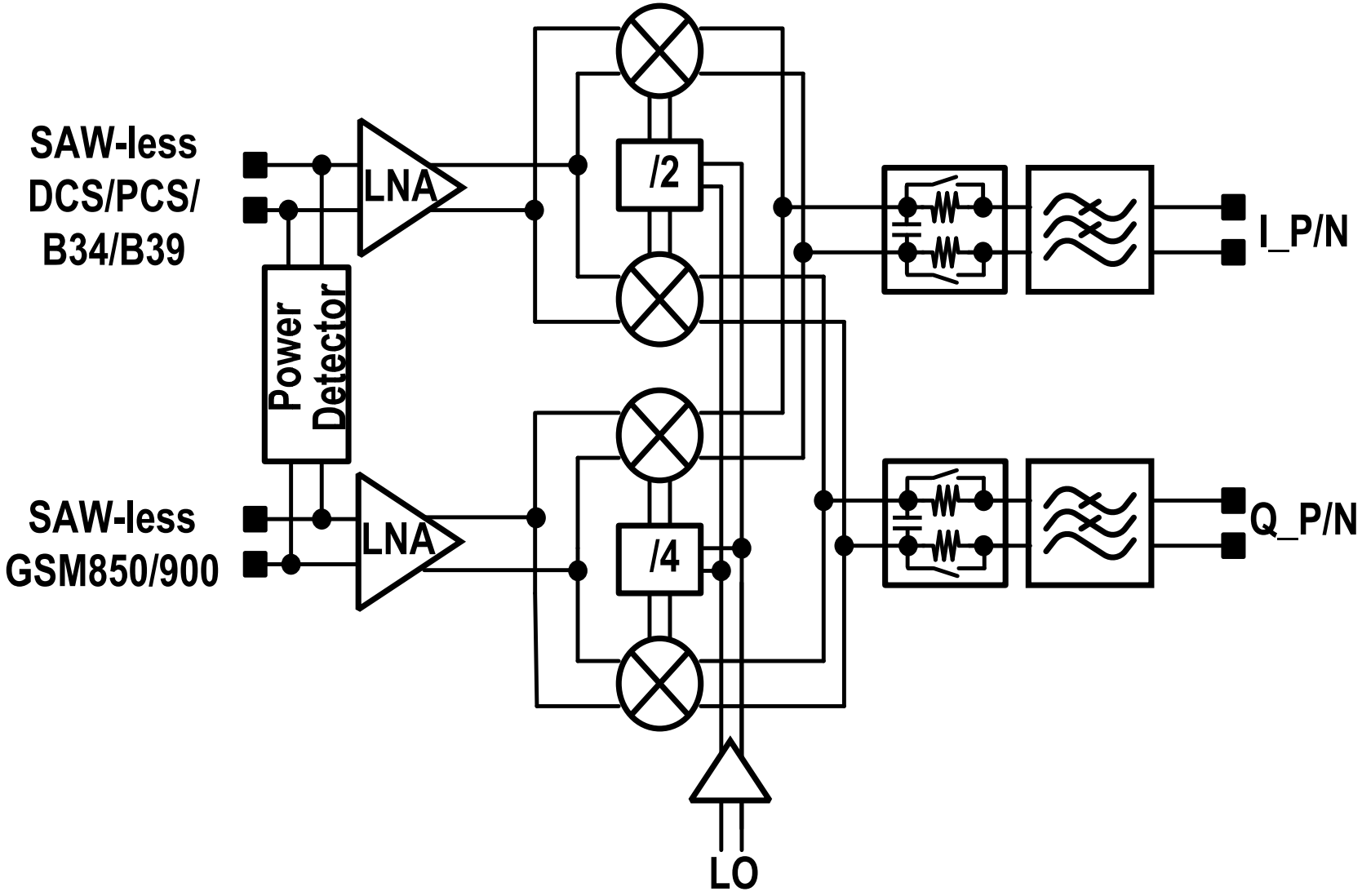
$\Rightarrow$

1. Signal desensitization
2. Blocker induced noise
3. LO phase noise/spur reciprocal mixing
4. Competitive power and area

Outline

- Architecture and Block Diagrams
- Circuit Overview
  - Inductor-less and current-mode noise-cancellation LNA
  - Adaptive RX and high selectivity interface for 2G/3G
  - Dynamic GBW-extension circuit technique
- Measurement Results
- Conclusion

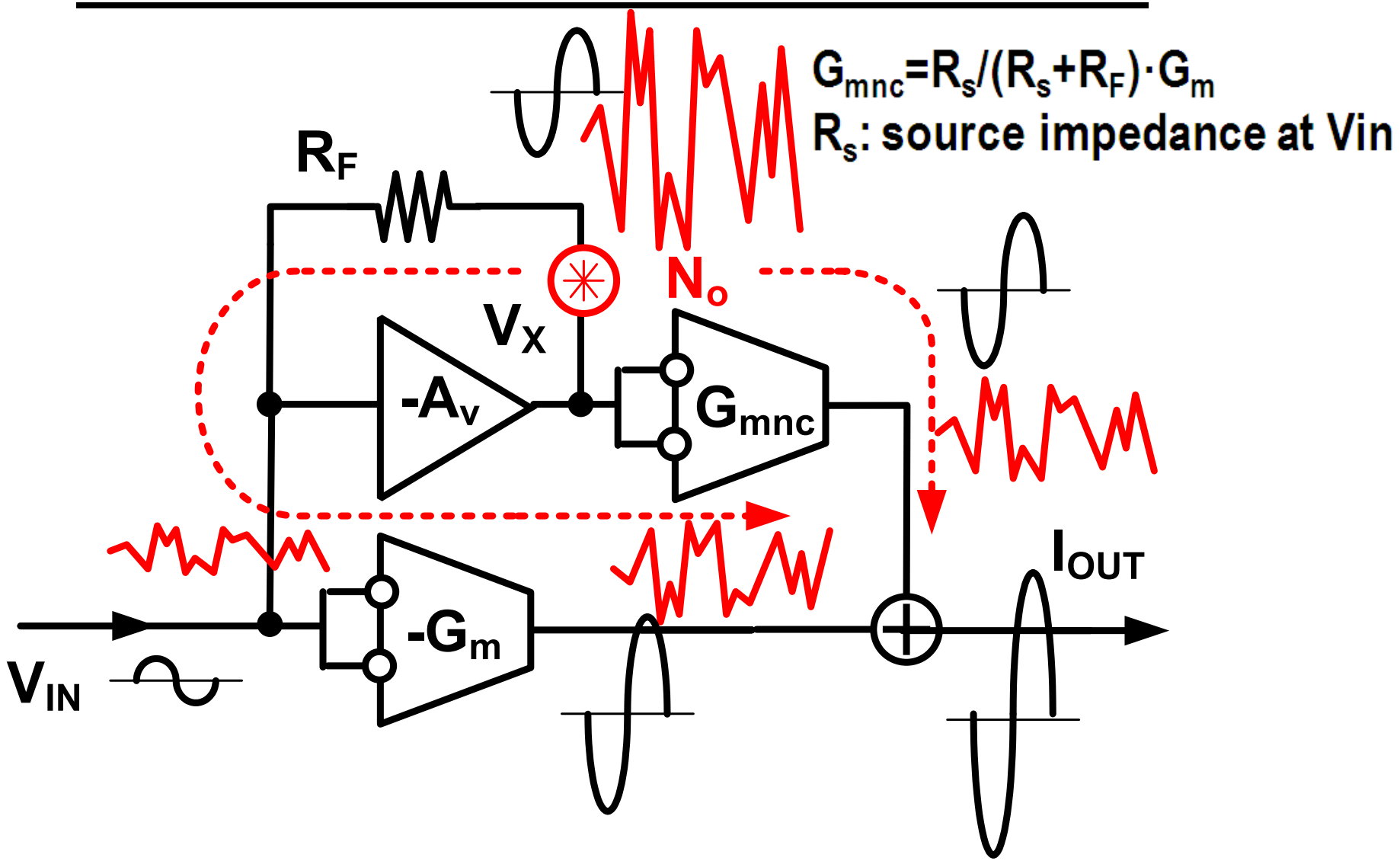
Receiver Block Diagram



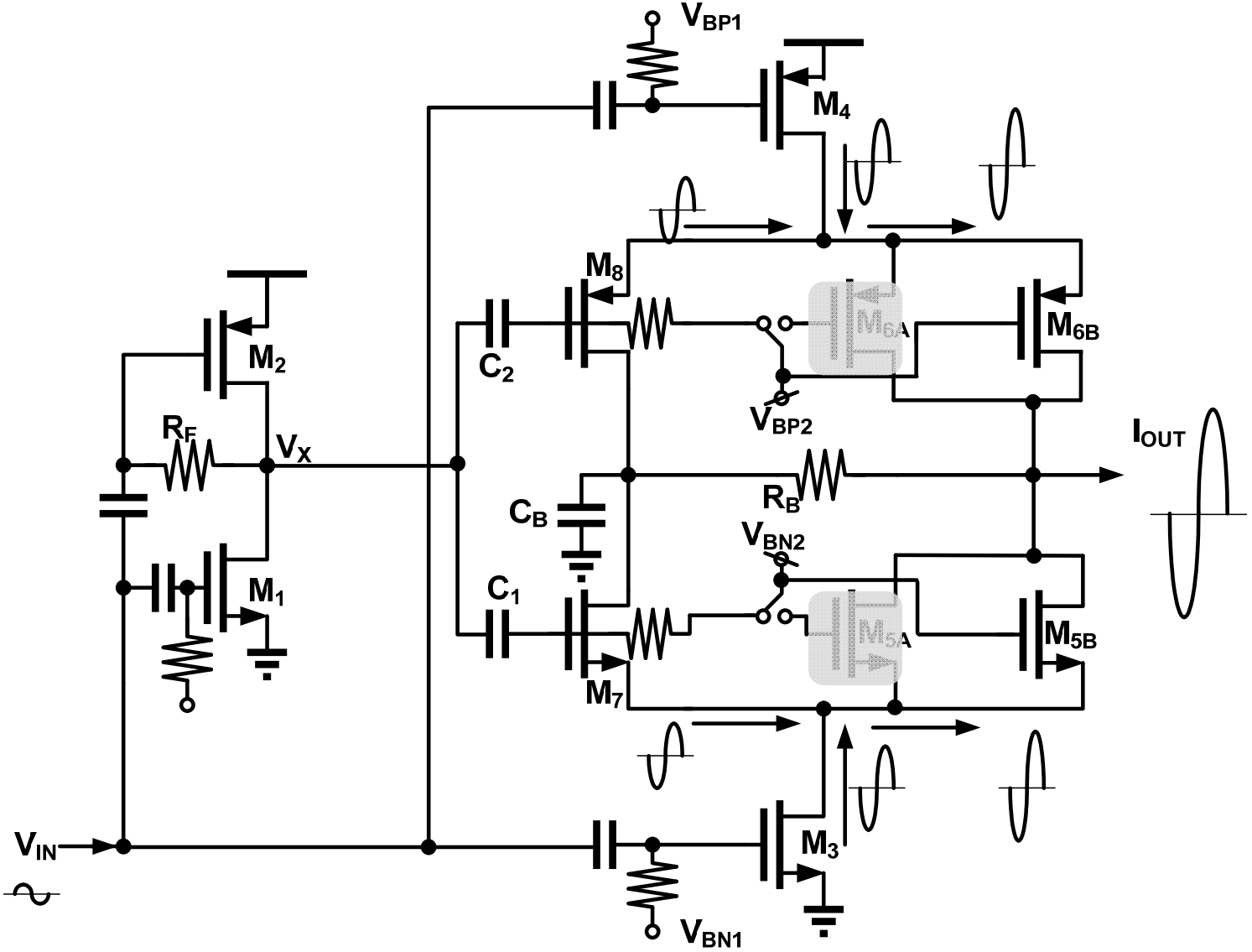
Outline

- Architecture and Block Diagrams
- Circuit Overview
  - Inductor-less and current-mode noise-cancellation LNA
  - Adaptive RX and high selectivity interface for 2G/3G
  - Dynamic GBW-extension circuit technique
- Measurement Results
- Conclusion

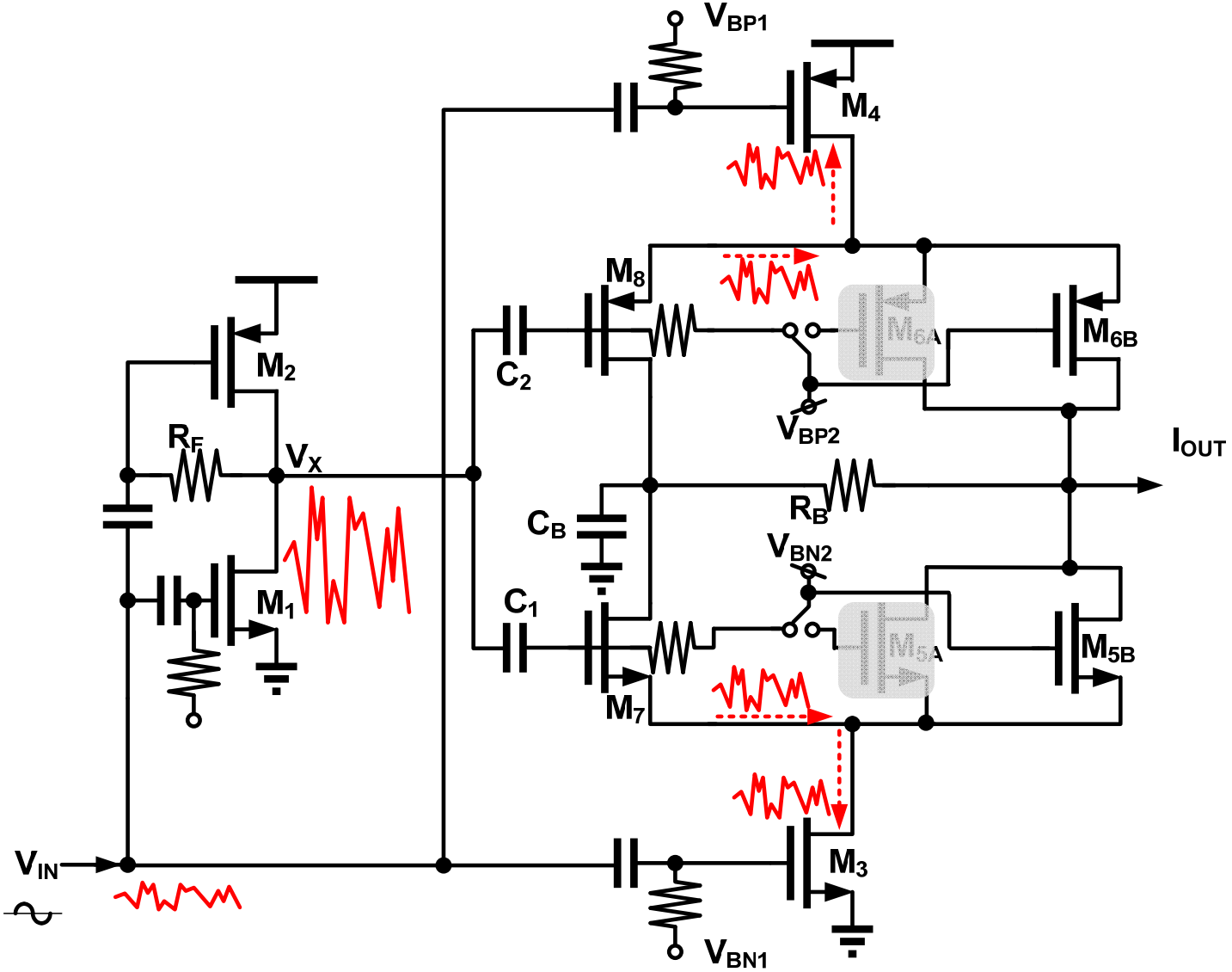
Inductor-less and Noise-cancellation LNA



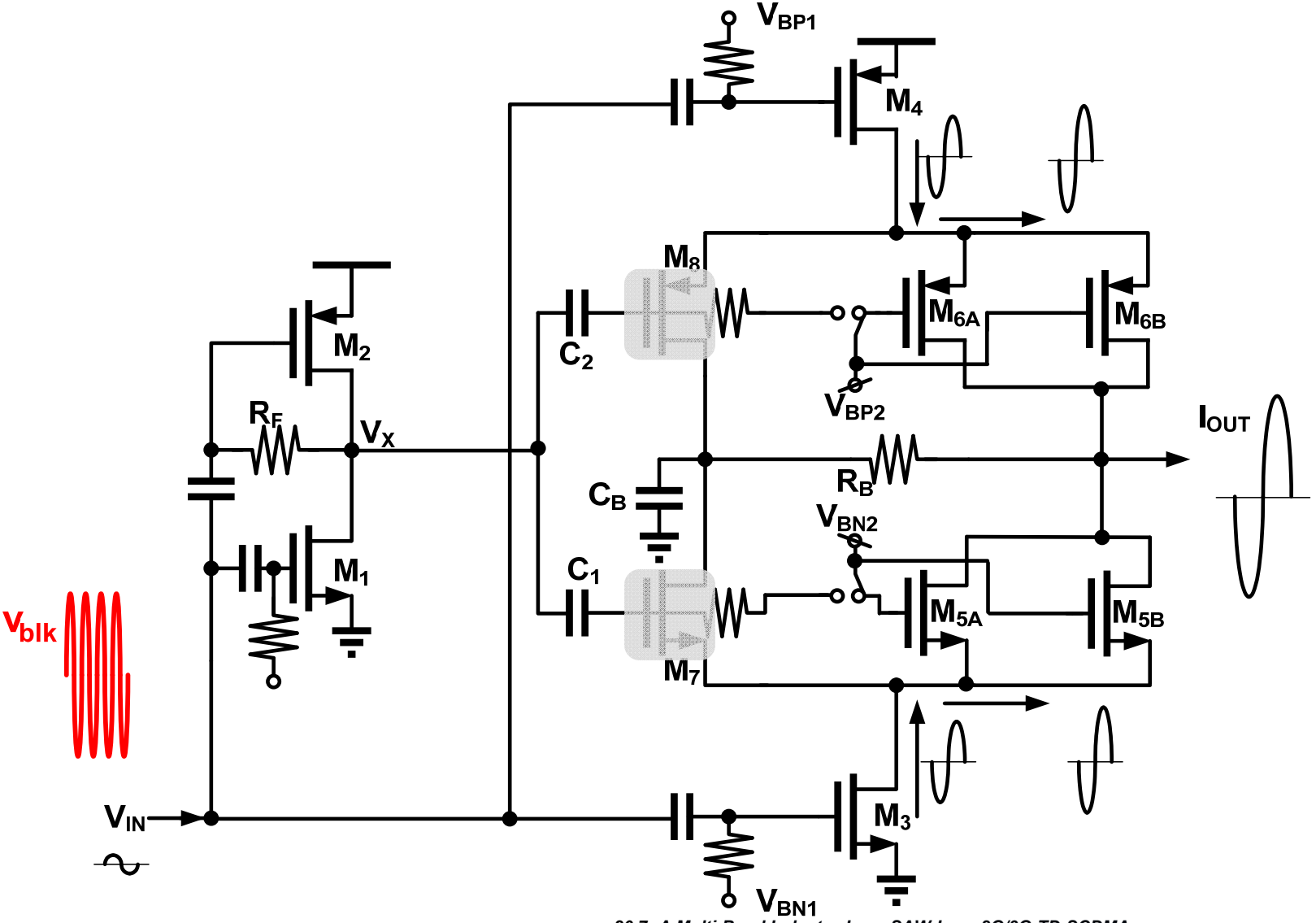
LNA Circuit Topology – Without OOB



LNA Circuit Topology – Without OOB



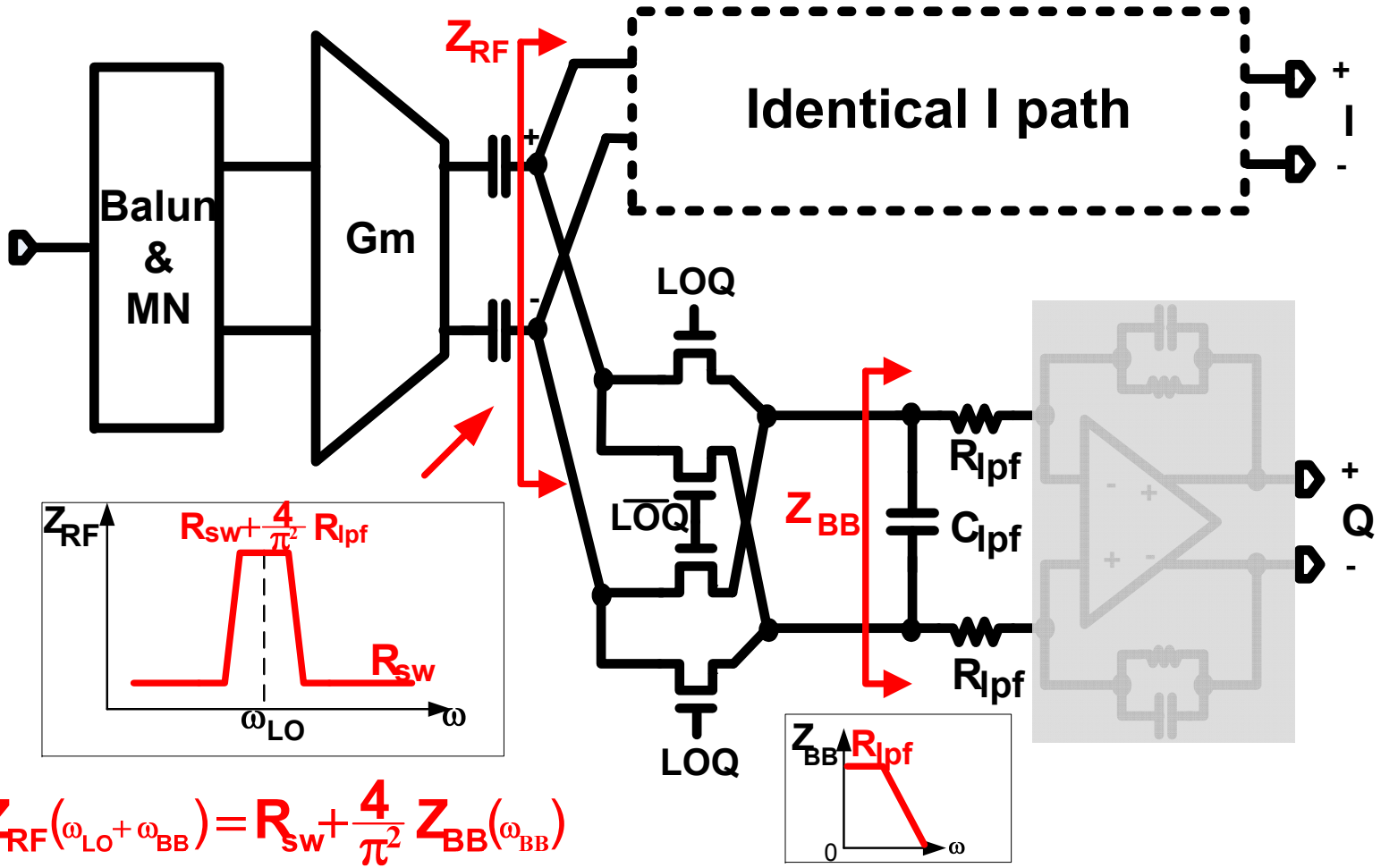
LNA Circuit Topology – With OOB



Outline

- Architecture and Block Diagrams
- Circuit Overview
  - Inductor-less and current-mode noise-cancellation LNA
  - Adaptive RX and high selectivity interface for 2G/3G
  - Dynamic GBW-extension circuit technique
- Measurement Results
- Conclusion

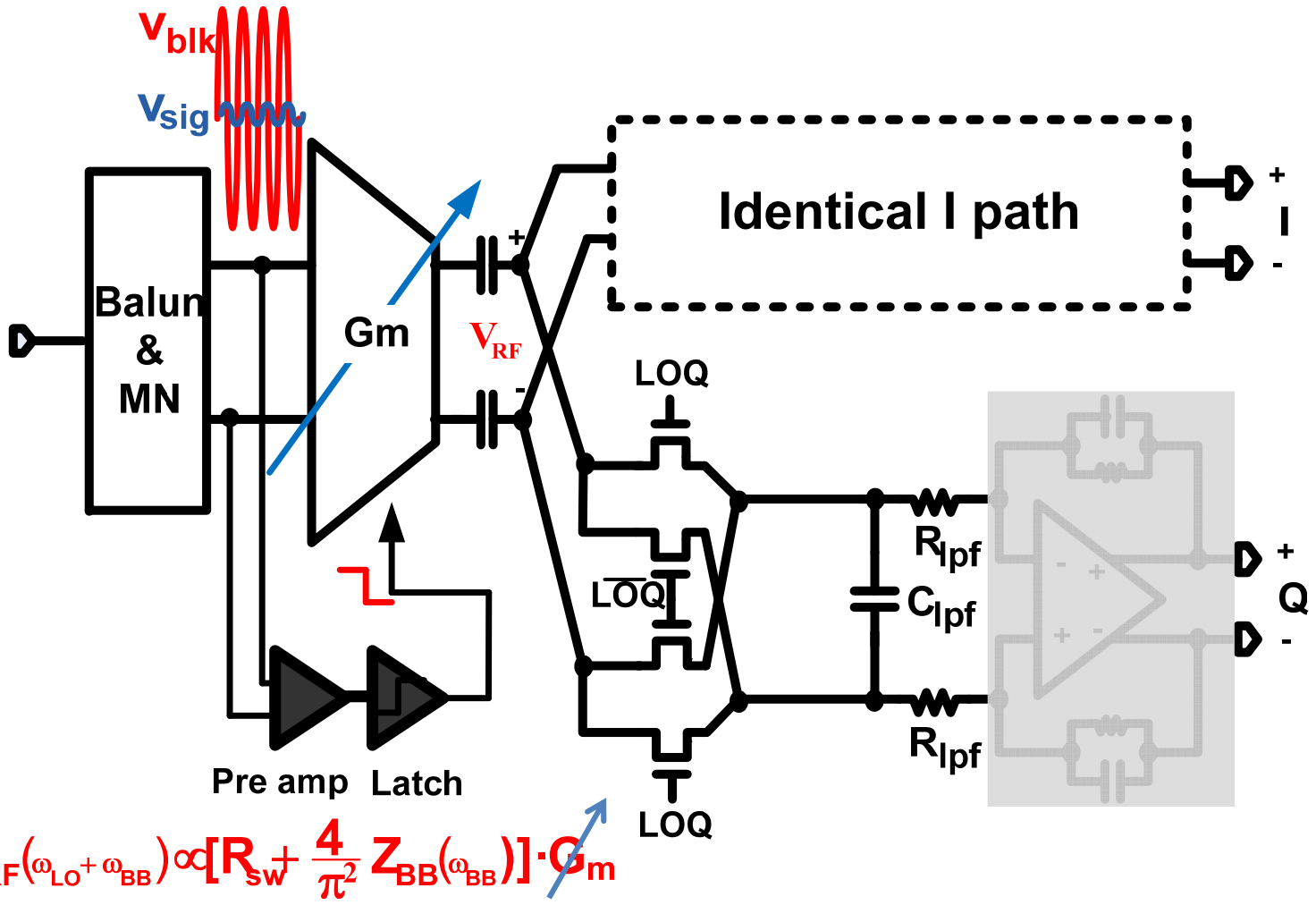
High Q Equivalent BPF



$$Z_{RF}(\omega_{LO}+\omega_{BB}) = R_{sw}+\frac{4}{\pi^2}Z_{BB}(\omega_{BB})$$

Z_{BB} at 20MHz offset is minimized by large C_{lpf} => trade-off with chip area

Slicing Gm for Out-of-band Blocker

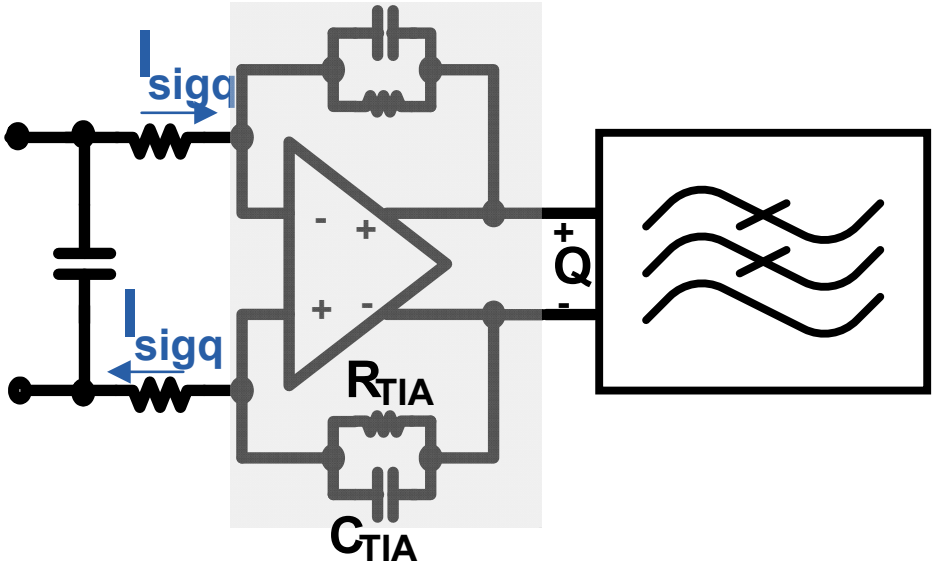


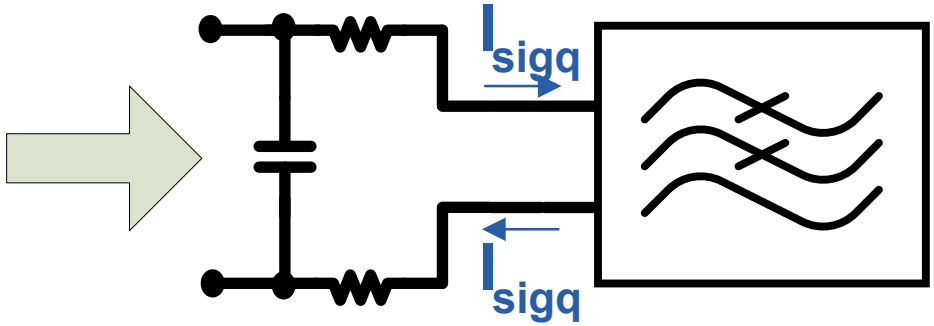
$$V_{RF}(\omega_{LO}+\omega_{BB}) \propto \left[R_{sw} + \frac{4}{\pi^2} Z_{BB}(\omega_{BB})\right] \cdot G_m$$

- Blocker-induced NF is dominated by LO reciprocal mixing.
- Slicing Gm can relax the C_{lpf} requirement for OOB and save chip area.

IF Interface

Trans-impedance amplifier (TIA)





- FE gain $\propto G_m \cdot R_{TIA}$
- R_{TIA} limited by FE gain partition
- C_{TIA} and OP occupy significant chip area !

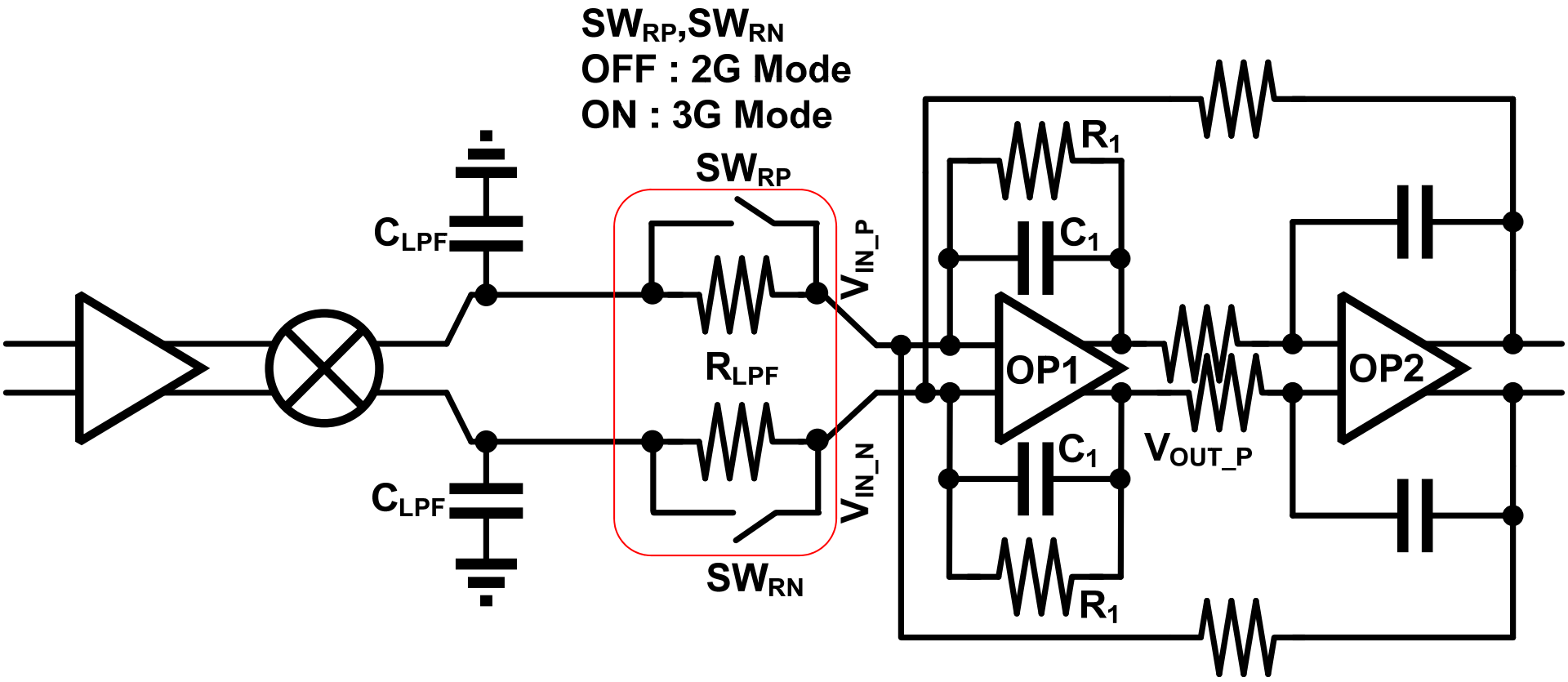
- Current-mode filter design
- Save TIA area and current

- CR filter for 2G OOB can cause 3G in-band drooping effect.

Outline

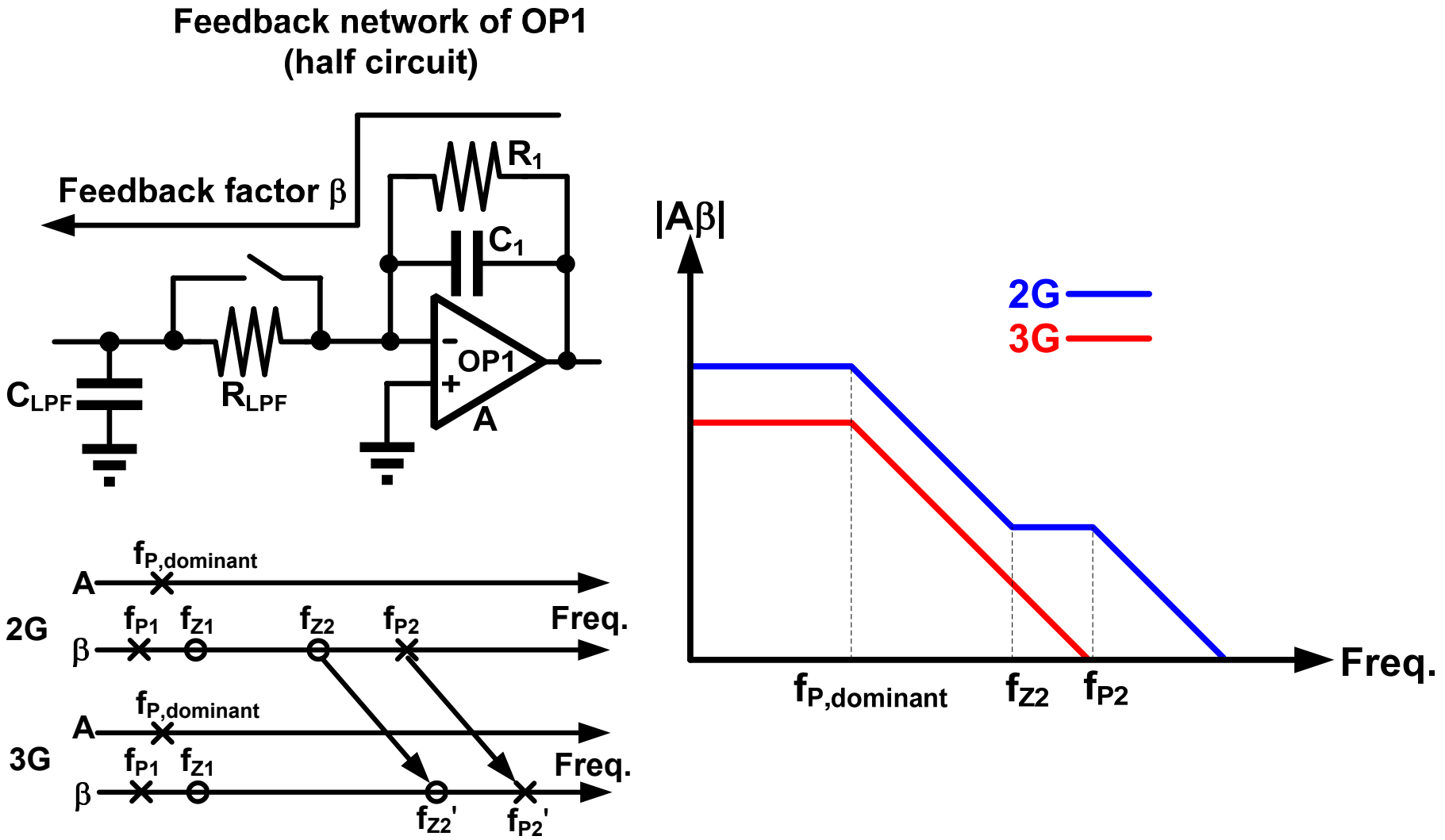
- Architecture and Block Diagrams
- Circuit Overview
  - Inductor-less and current-mode noise-cancellation LNA
  - Adaptive RX and high selectivity interface for 2G/3G
  - Dynamic GBW-extension circuit technique
- Measurement Results
- Conclusion

Programmable CR Filter



- Programmable R_{LPF} by turning on SW_{RP} and SW_{RN}

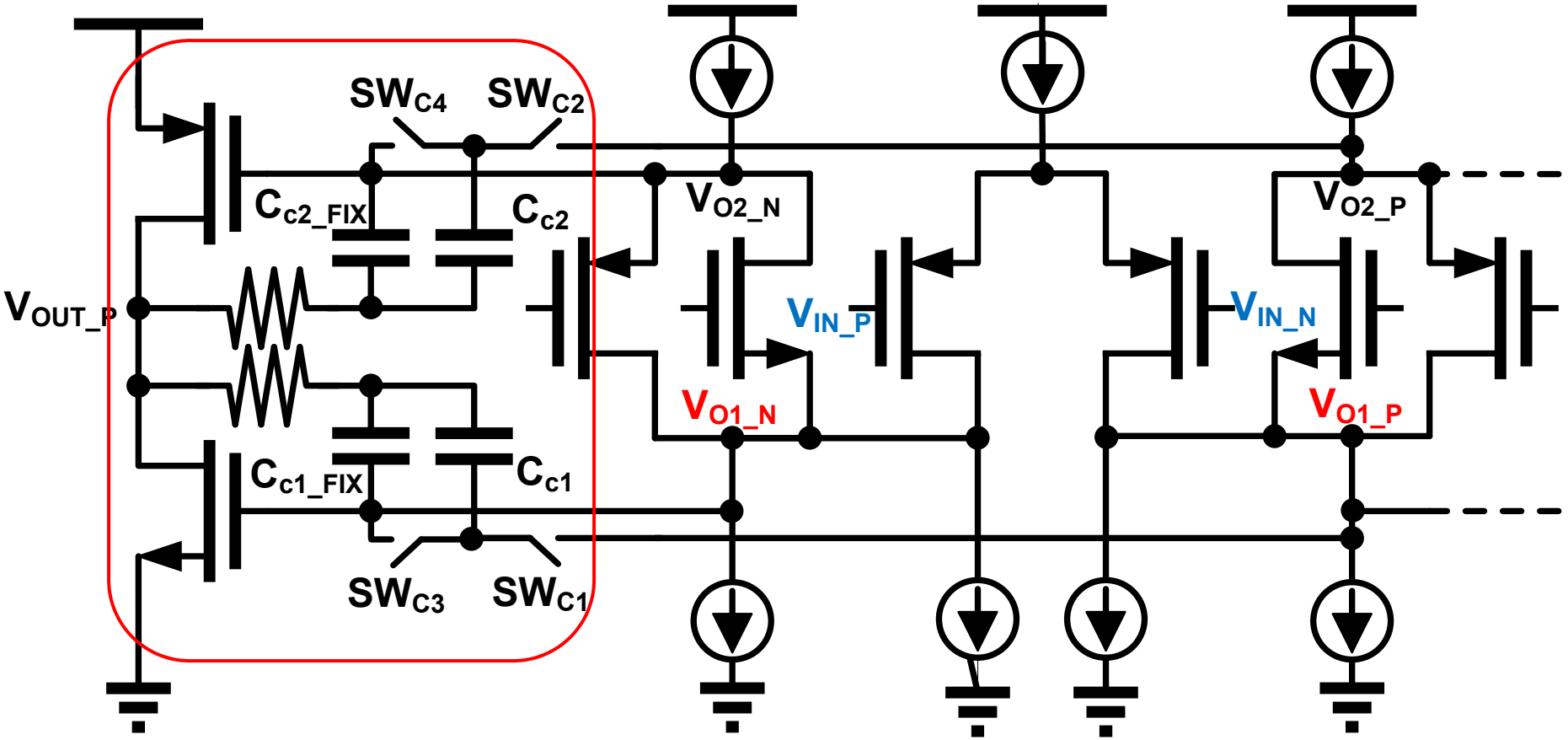
IF OP1 Loop GBW Problem in 3G



(f_{P1} and f_{Z1} occur close together and thus counteract each other)

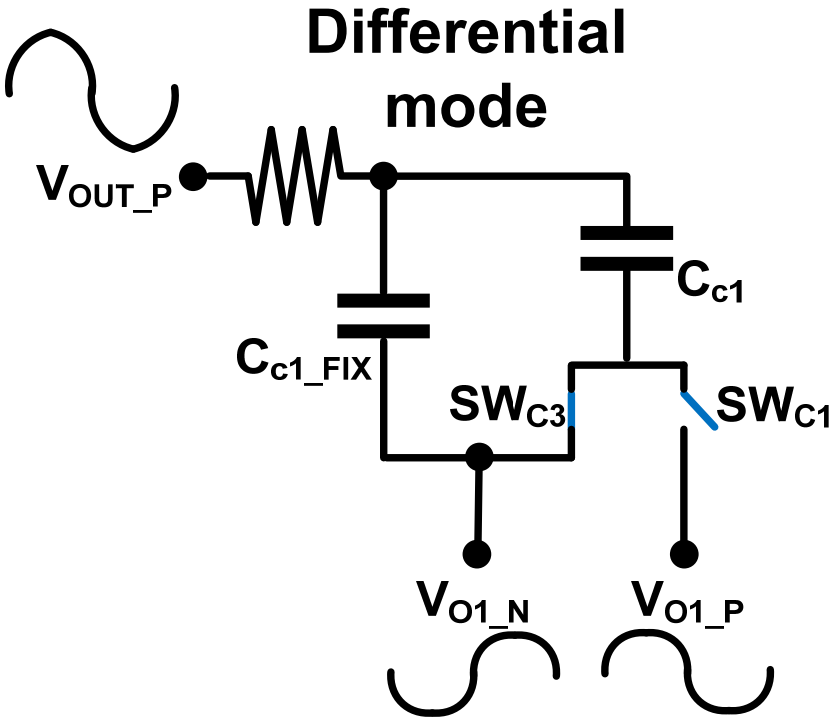
Dynamic loop GBW extension technique

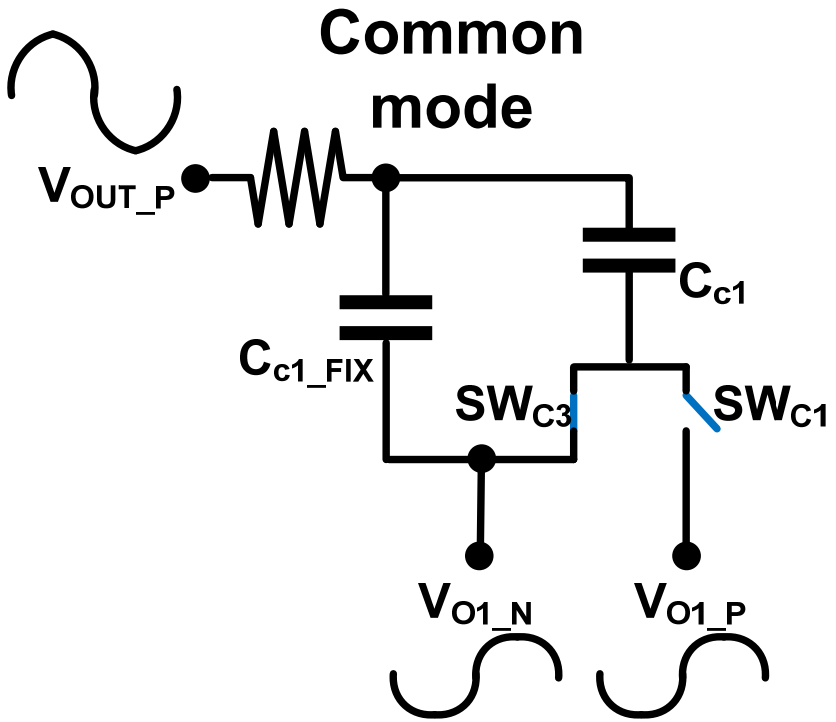
OP1 (simplified schematic)



- 2G mode : $SW_{C1/C2}$ off, $SW_{C3/C4}$ on
- 3G mode : $SW_{C1/C2}$ on, $SW_{C3/C4}$ off

Dynamic loop GBW extension technique





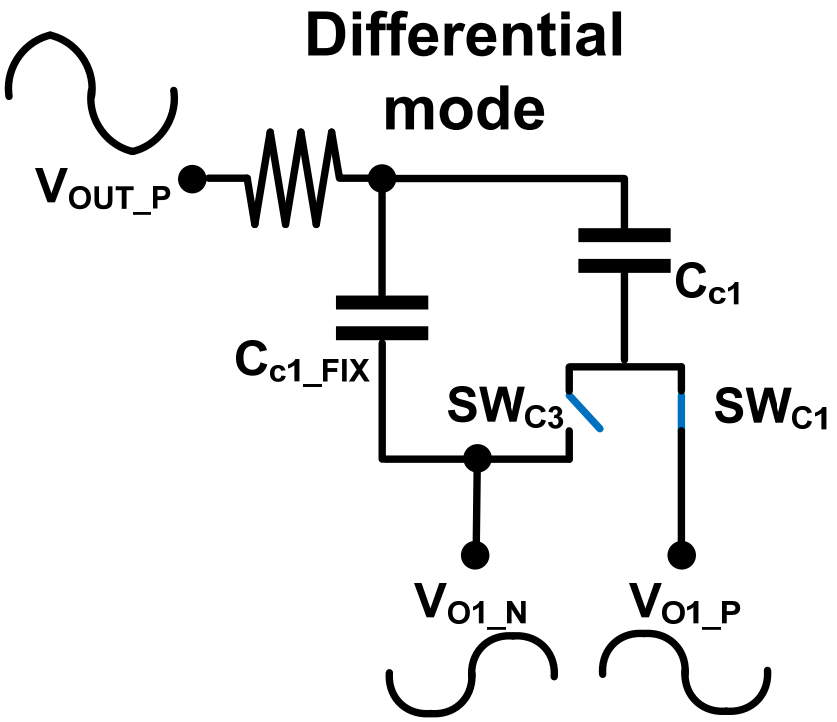
2G mode (SW_{C1} off, SW_{C3} on)

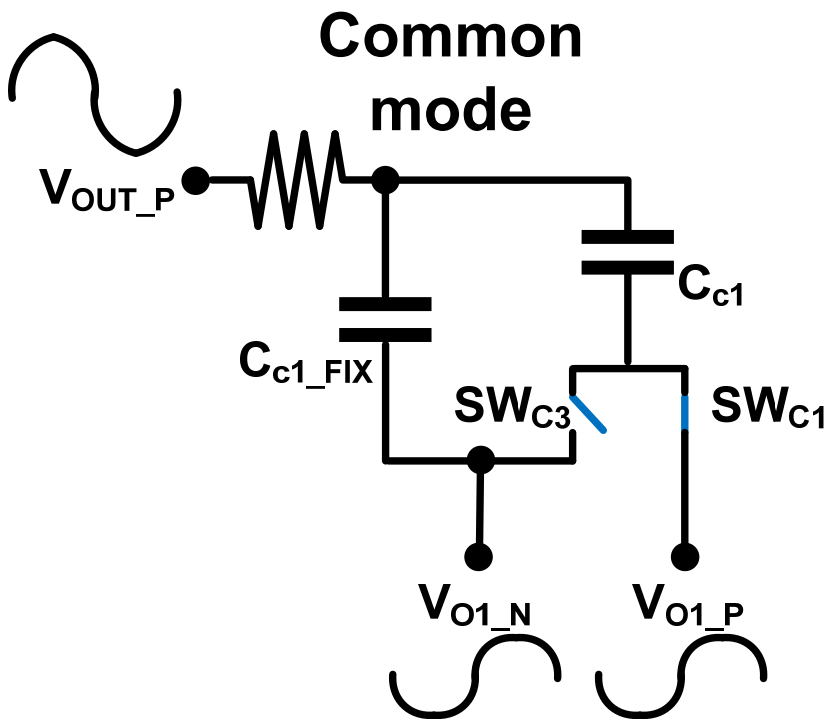
$\rightarrow C_{c1\_diff,\ 2G} = C_{c1\_FIX} + C_{c1}$

2G mode (SW_{C1} off, SW_{C3} on)

$\rightarrow C_{c1\_com,\ 2G} = C_{c1\_FIX} + C_{c1}$

Dynamic loop GBW extension technique





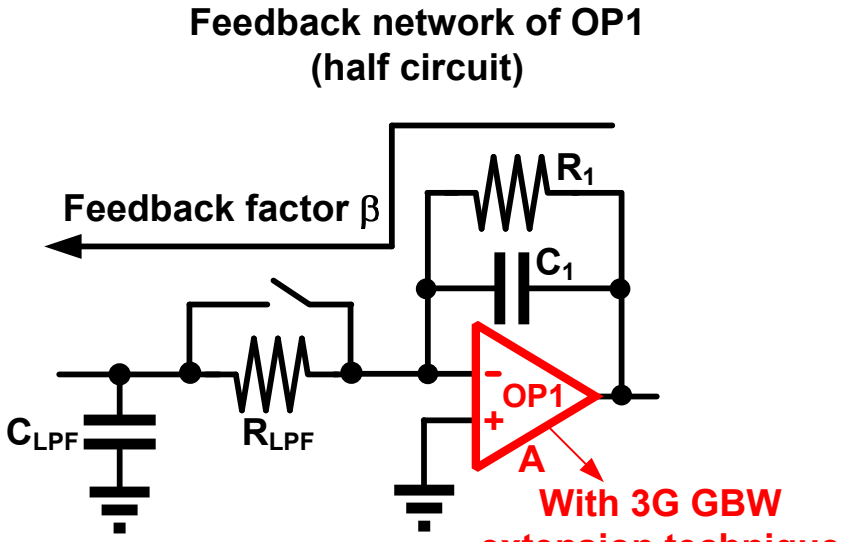
3G mode (SW_{C1} on, SW_{C3} off)

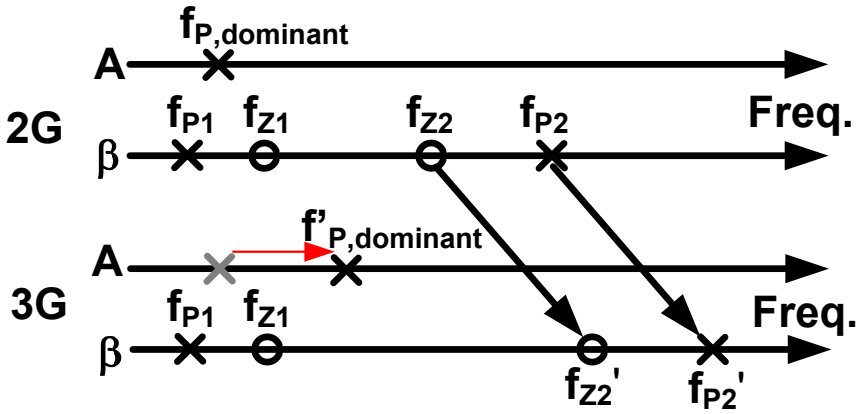
→ $C_{c1\_diff,\ 3G} = C_{c1\_FIX} - C_{c1}$

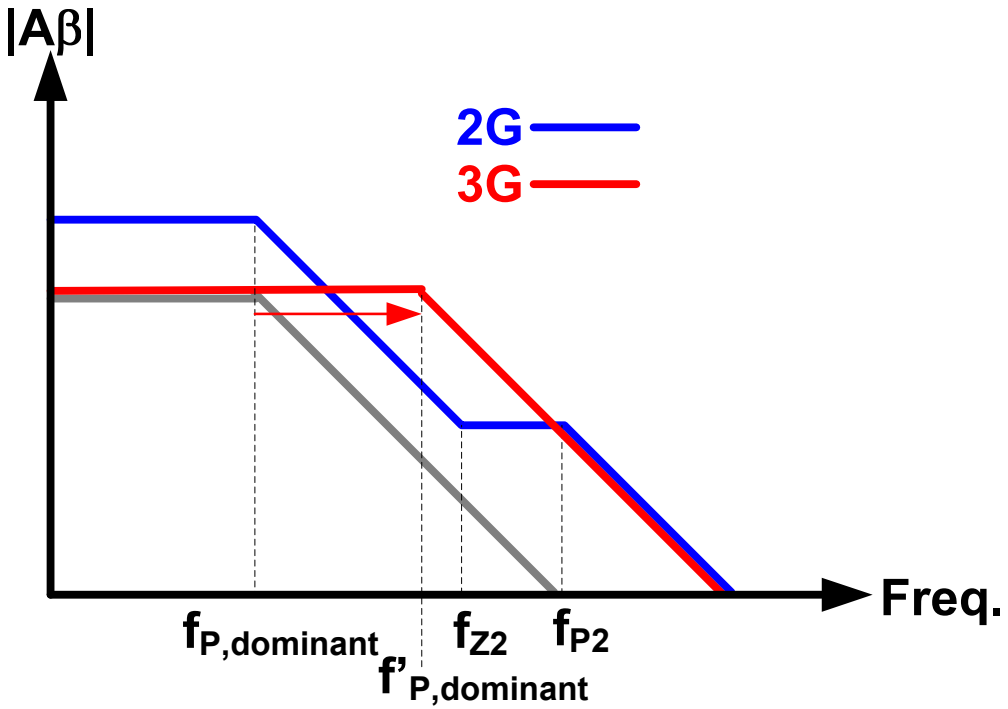
3G mode (SW_{C1} on, SW_{C3} off)

→ $C_{c1\_com,\ 3G} = C_{c1\_FIX} + C_{c1}$

Dynamic loop GBW extension technique





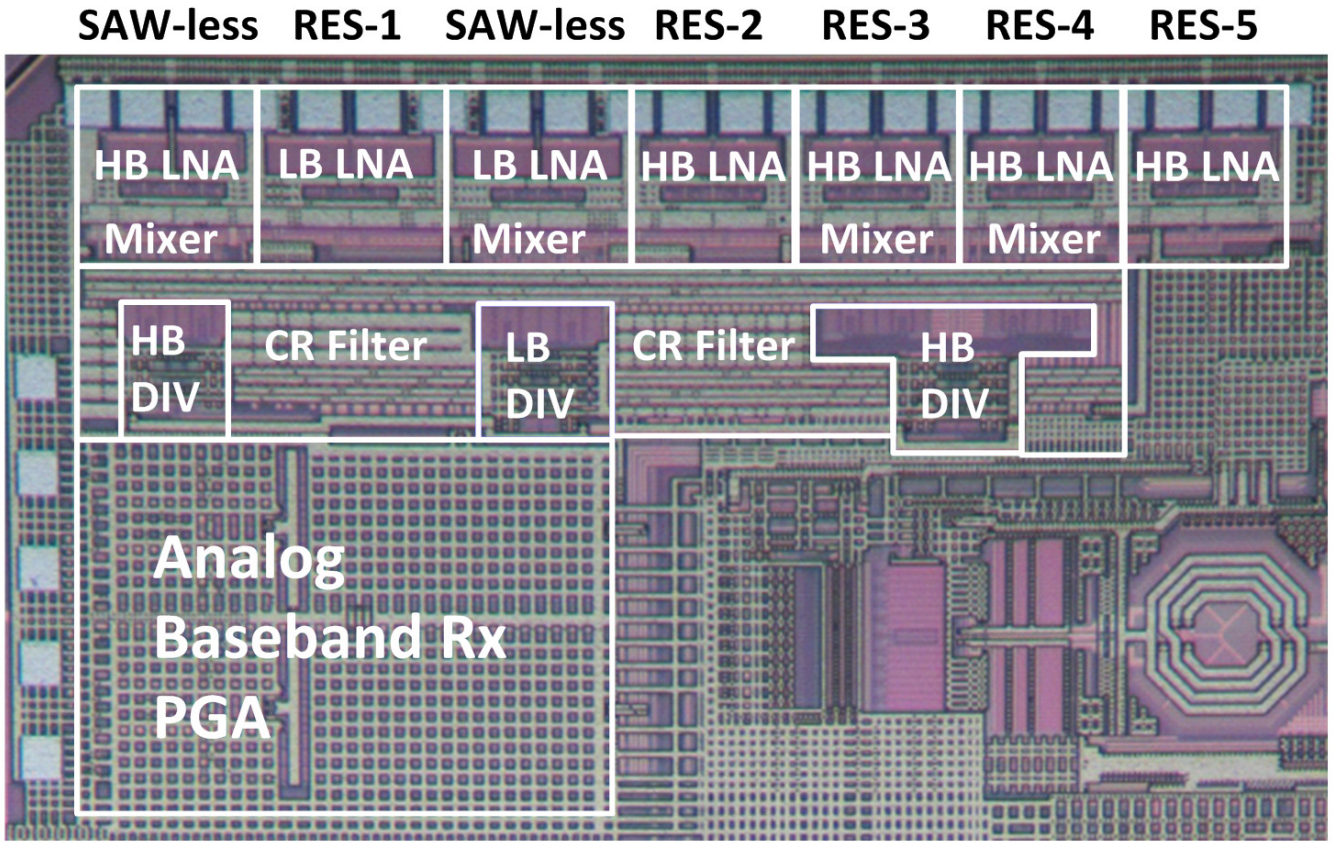


(f_{P1} and f_{Z1} occur close together and thus counteract each other)

Outline

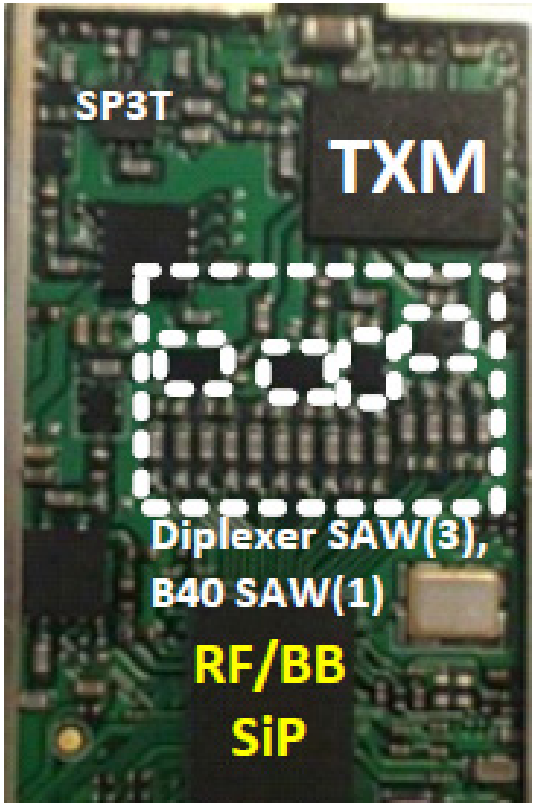
- Architecture and Block Diagrams
- Circuit Overview
  - Inductor-less and current-mode noise-cancellation LNA
  - Adaptive RX and high selectivity interface for 2G/3G
  - Dynamic GBW-extension circuit technique
- Measurement Results
- Conclusion

Die Photo

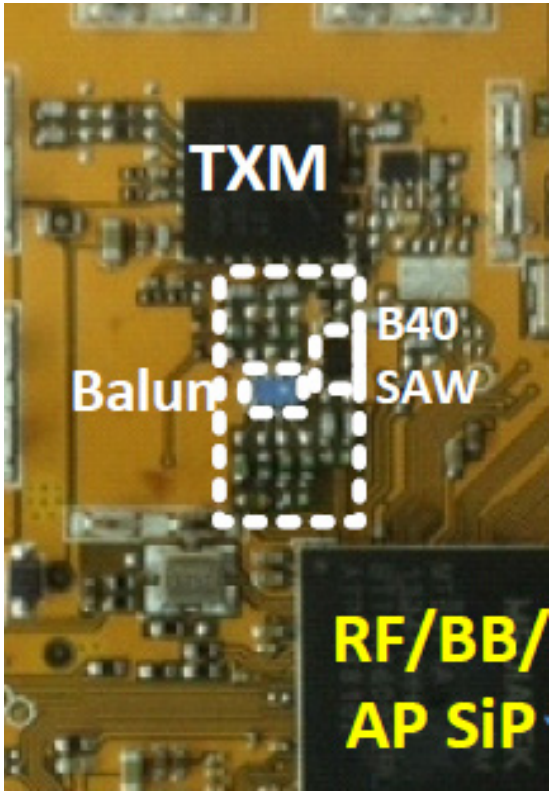


- 40nm CMOS
- RX chip area : 0.57 mm^2 including IF filter

Reference Phone Board

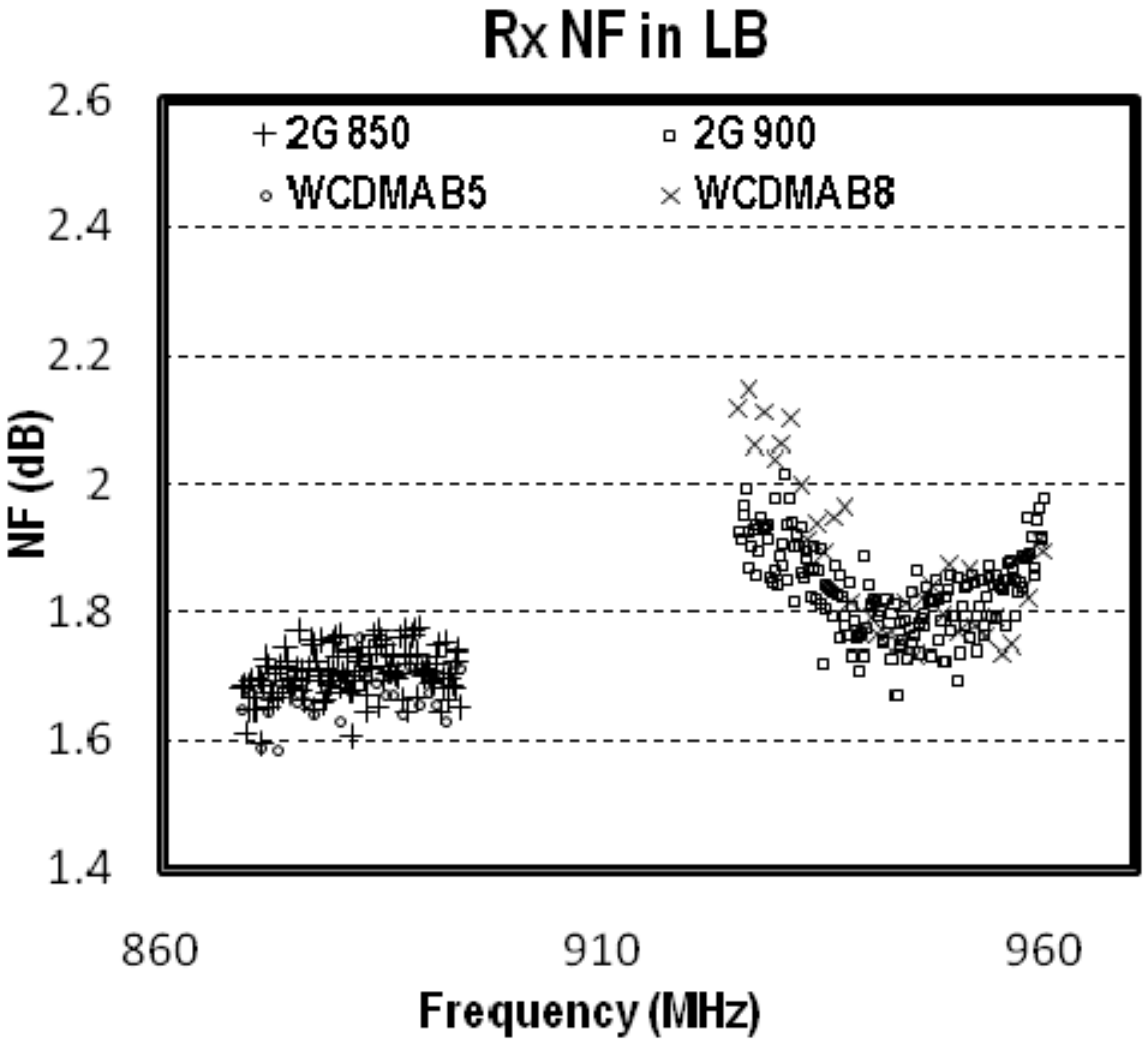


Conventional Quad Band GSM/EDGE & TD-SCDMA RX



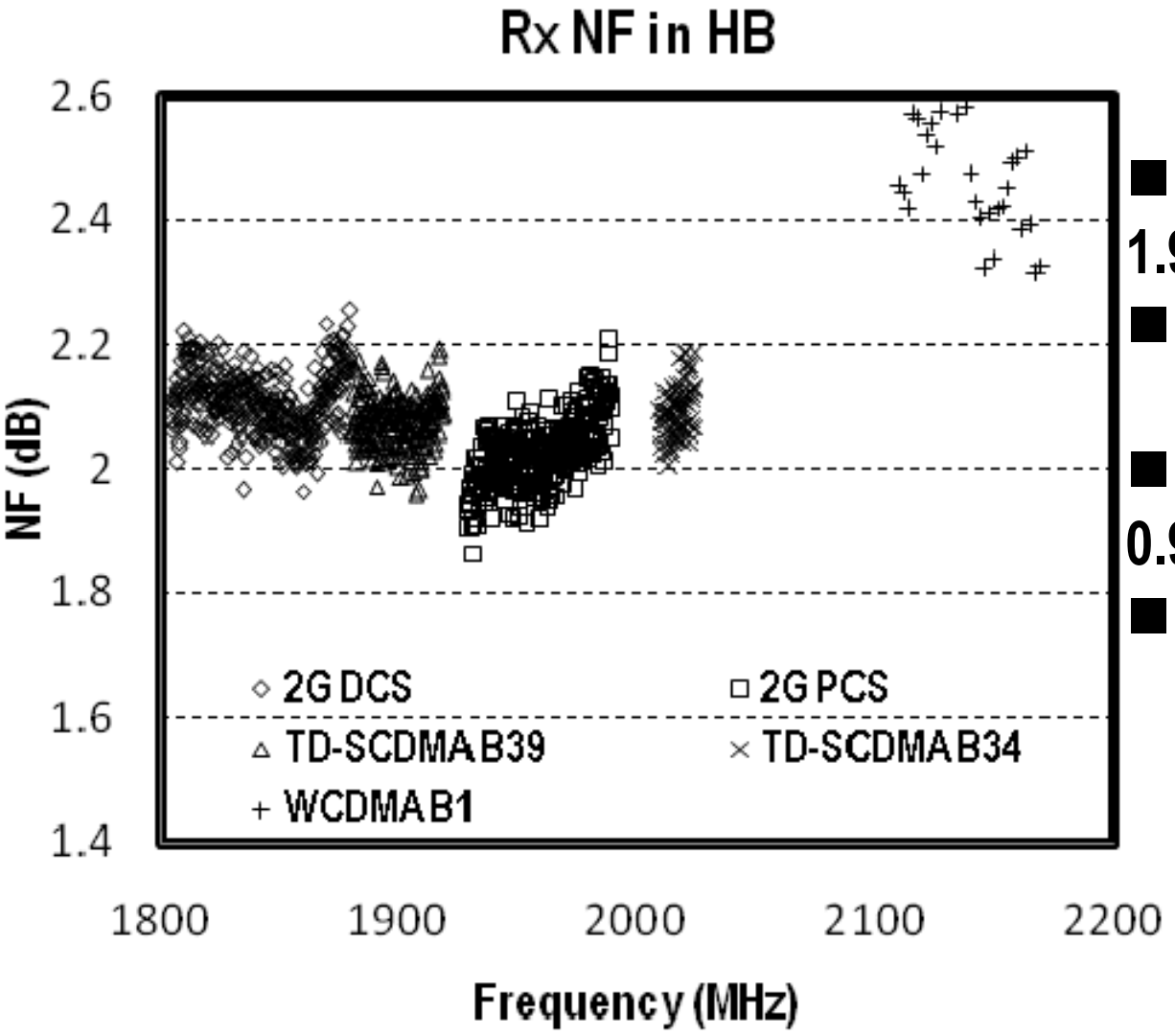
SAW-less RX

RX LB Noise Figure



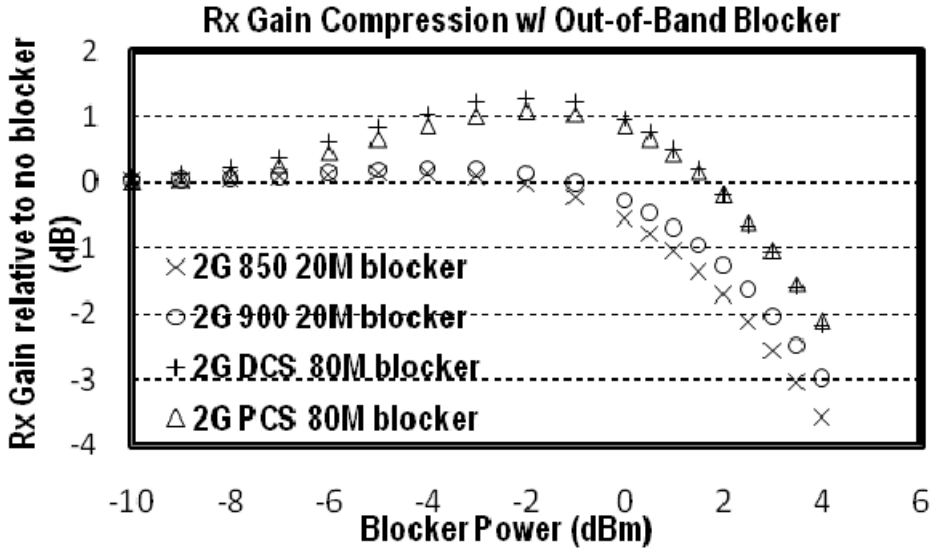
- NF at GSM850 & B5 : ~1.7dB
- NF at GSM900 & B8 : 1.7 – 2.1dB
- WCDMA IF BW : 2.3MHz

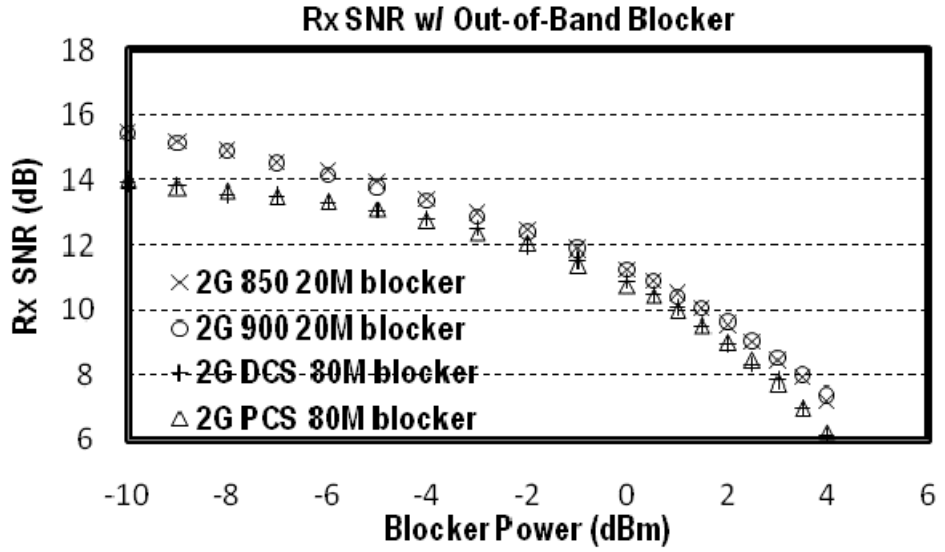
RX HB Noise Figure



- NF at DCS/PCS/B34/B39: 1.9 – 2.2dB
- NF at B1: ~ 2.4dB
- TD-SCDMA IF BW : 0.95MHz
- WCDMA IF BW : 2.3MHz

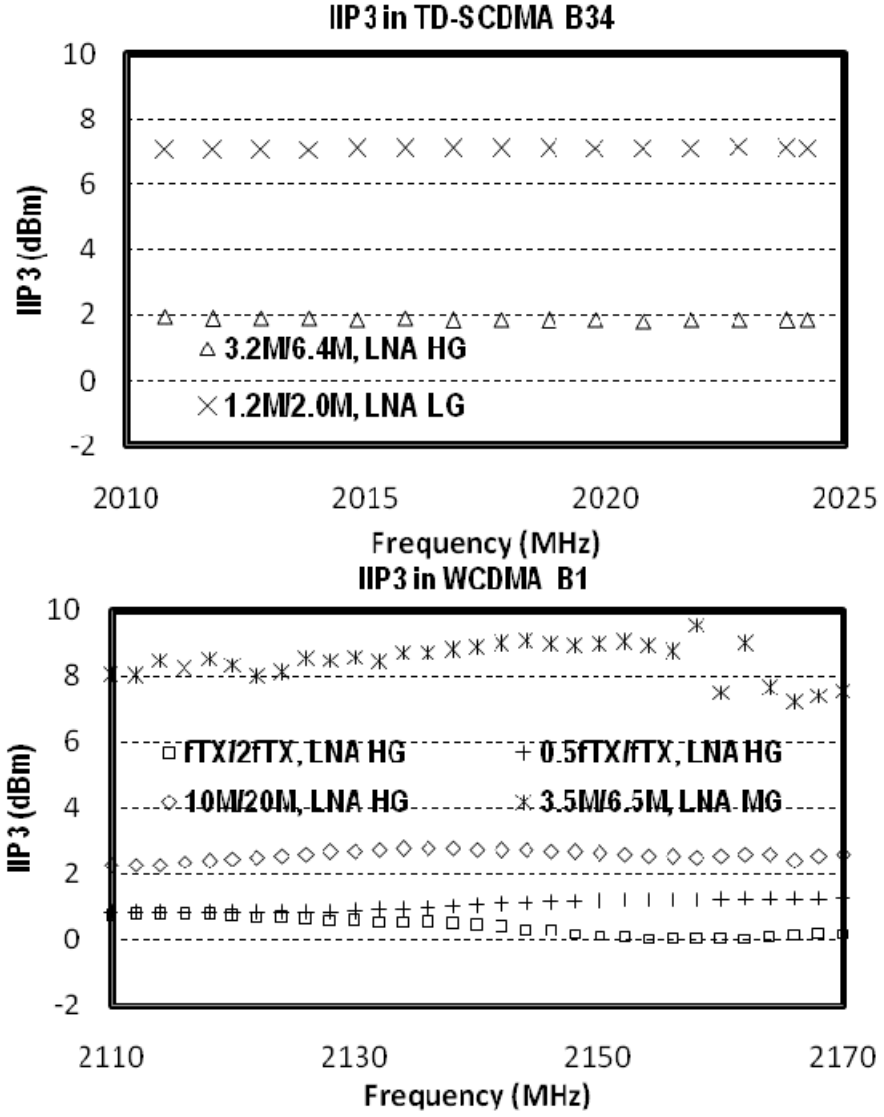
P_{1dB} and SNR with OOB





- In-band signal : -99dBm
- >0dBm 20M/80M-offset blockers for 2G LB/HB
- 15 dB more relaxed for TD-SCDMA
- Whole system SNR > 7.7 dB up to +3dBm blocker

Linearity - IIP3



- TD-SCDMA IF BW : 0.95MHz
- In-band IIP3 > +1.9 / +7 dBm @ LNA HG / LG mode

- WCDMA IF BW : 2.3MHz
- B1 IIP3 : +0.4 / +8.5 dBm @ LNA HG / MG mode

Measurement Summary

	ISSCC 2011[1]	ISSCC 2011 [3]	ISSCC 2012 [4]	ISSCC 2013 [5]	This work
Process	65nm CMOS	65nm CMOS	40nm CMOS	40nm CMOS	40nm CMOS
Need Rx SAW Filter	YES	NO	NO	NO	NO
On-Chip Inductor	NO	YES	NO	YES	NO
Number of LNAs	8	2	1	1	7
Applications	GSM/EDGE/WCDMA	GSM/EDGE	N/A	N/A	GSM/EDGE/TD-SCDMA/WCDMA
Rx Gain (dB)	67	60	70	45.5	57
Rx NF (dB)	2.5/2.4	2.7/2.9	1.9	1.9	1.7/1.8/2.1/2.4
Rx Out-of-Band P_{1dB} (dBm)	N/A	1	>0	–1	>2
Rx NF with 0dBm Out-of-Band blocker	N/A	8.5/7.0	4.1	7.9	11
Out-of-Band IIP3 (dBm) ($f_{Tx}/2f_{Tx}$)	–3	>0	13.5	16	0.4
In-Band IIP3 (dBm) 10M/20M, LNA HG 3.2M/6.4M, LNA HG 3.5M/6.5M, LNA MG	 -3 N/A 4	 N/A N/A N/A	 10 -20 N/A	 N/A N/A N/A	 2.6 1.9 8.5
Out-of-Band IIP2 (dBm)	>50	>50	54	66	>55
Supply Voltage (V)	1.5	1.4/2.5	1.3	1.2/1.8	1.5
Rx Current (mA)	38.5*	37.1	27~60#	19.5	26/31
Area (mm^2)	0.88 (w/o IF filter)	1.05 1.4(w/ IF filter)	1.2 (w/o IF filter)	0.74 (w/o IF filter)	0.42 0.57(w/ IF filter)

*: using a DC-DC converter[1].

#: The LO path consumes 3 to 36 mA, the RF GM cell draws 8mA, and the baseband circuits consume 16mA[4].

Outline

- Architecture and Block Diagrams
- Circuit Overview
  - Inductor-less and current-mode noise-cancellation LNA
  - Adaptive RX and high selectivity interface for 2G/3G
  - Dynamic GBW-extension circuit technique
- Measurement Results
- Conclusion

Conclusion

- SAW-Less RX requires a high dynamic range frontend, while meeting noise and current consumption specifications
  - Inductor-less and current-mode noise-cancellation LNA
  - Adaptive RX and high selectivity interface for 2G/3G
  - Dynamic GBW-extension circuit technique
- The most compact triple-mode and six-band TDD cellular receiver among the state-of-the-art receivers listed in the Table.

Paper 20.8

A 20mW GSM/WCDMA Receiver with RF Channel Selection

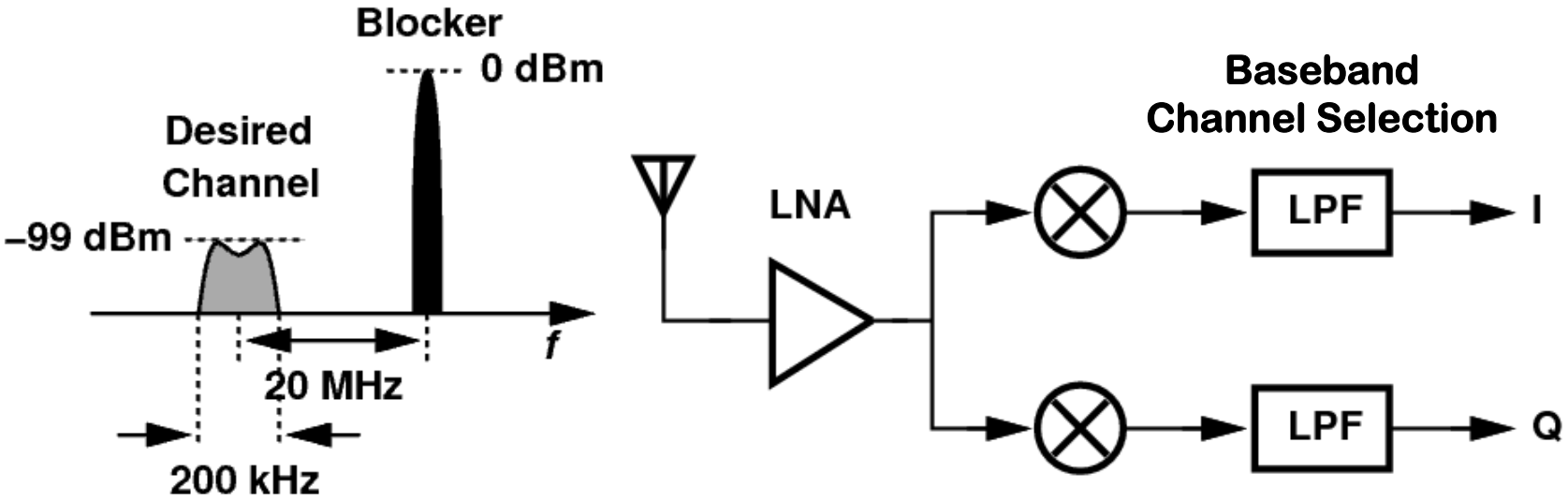
Joung Won Park and Behzad Razavi

Electrical Engineering Department
University of California, Los Angeles

Outline

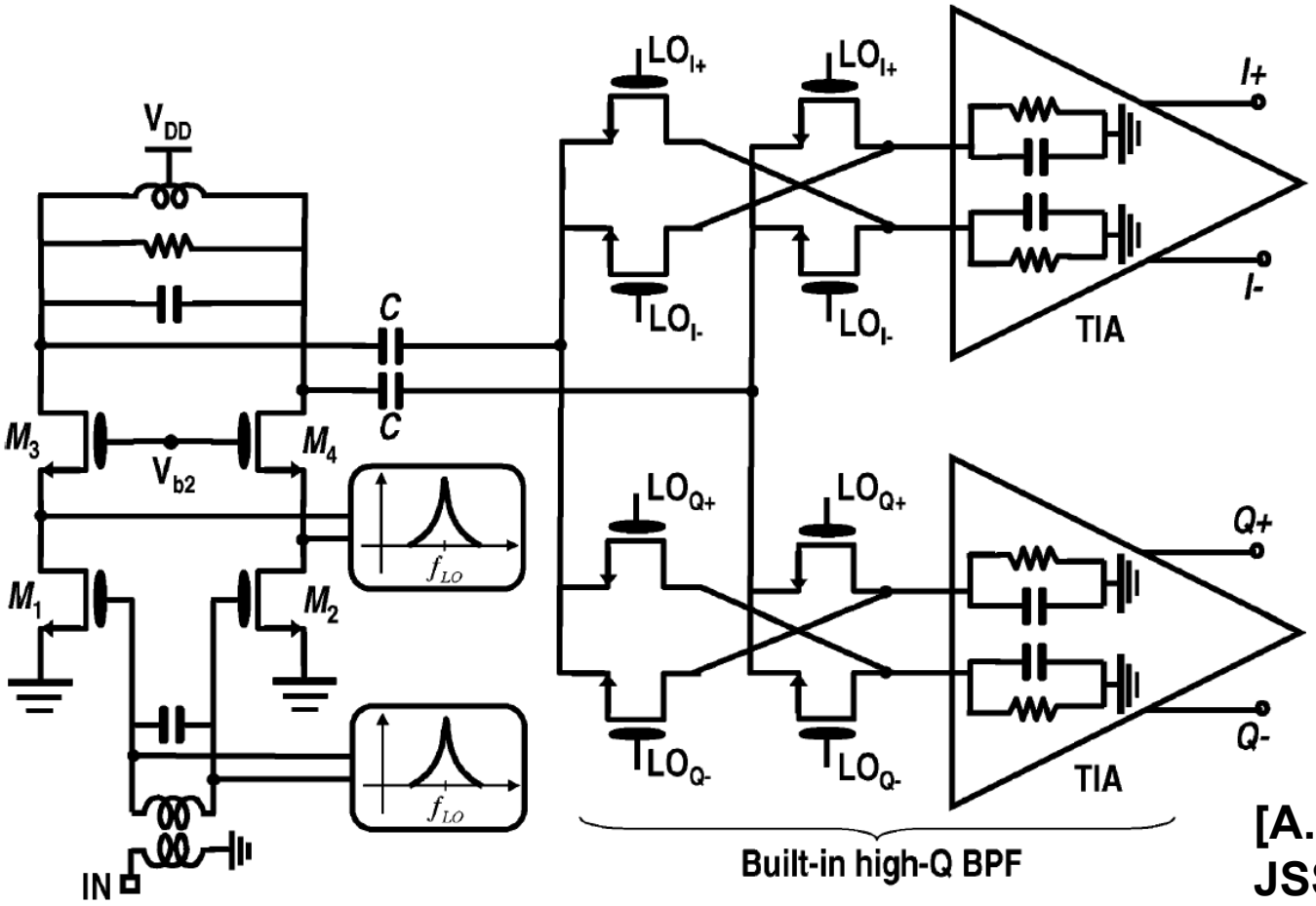
- Introduction
- Proposed Concepts:
  - Miller Notch Filter and Its Variants
  - Receiver Architecture
  - Broadband Noise Rejection
- Experimental Results
- Conclusion

The GSM Challenge



- **Channel selection at RF:**
  → Linearity of <u>all</u> subsequent circuits is relaxed.
- **But how?**

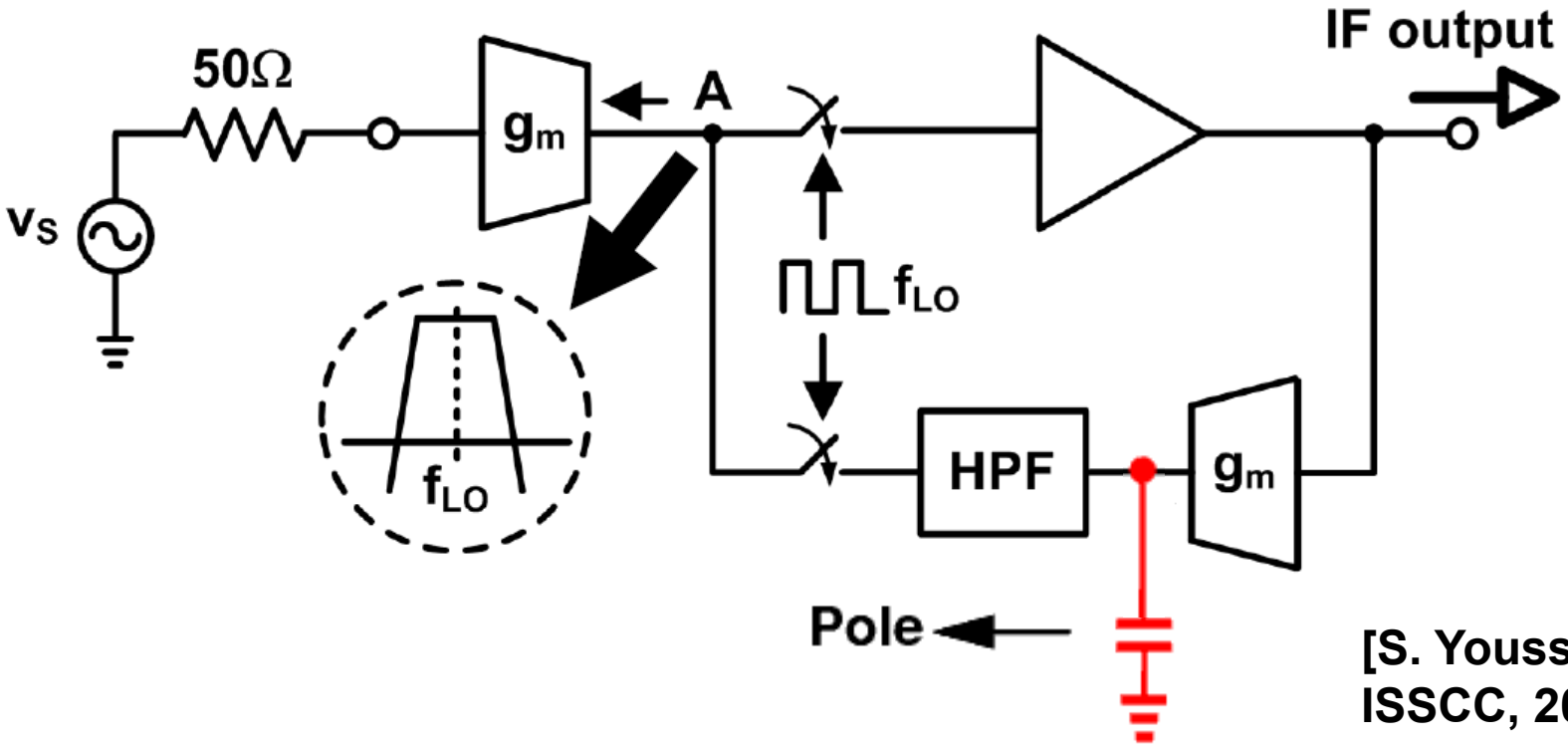
Example of Prior Art (I)



[A. Mirzaei et al, JSSC, Apr. 11]

- 3-dB bandwidth = 14 MHz
- Total cap = 440 pF
- NF with a 0-dBm blocker at 80-MHz offset = 11.4 dB

Example of Prior Art (II)

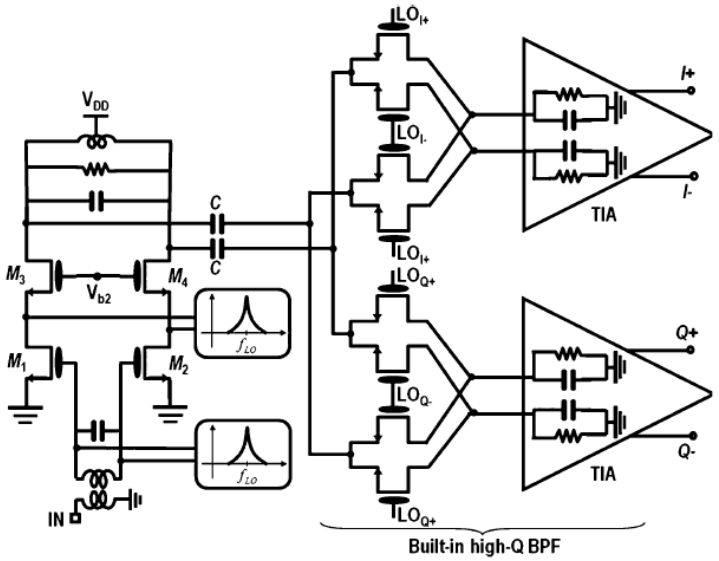


[S. Youssef et al, ISSCC, 2012]

- 3-dB bandwidth = 5 MHz
- Poor input matching
- No blocker test
- Feedback pole destabilizes the loop.
  → Power consumption = 62 mW

What would it take to satisfy GSM?

Mirzaei et al

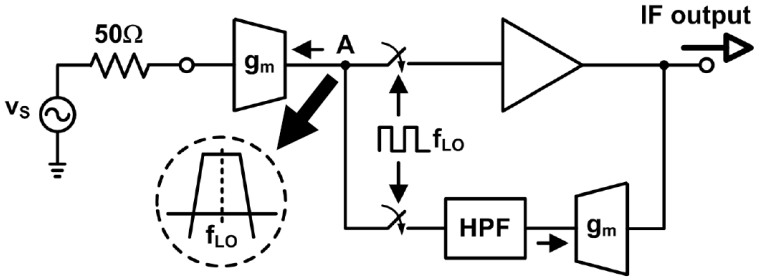


GSM

C_{tot} = 30 nF

P_{tot} = ?

Youssef et al



GSM

C_{tot} = 1.5 nF

P_{tot} = 150 mW

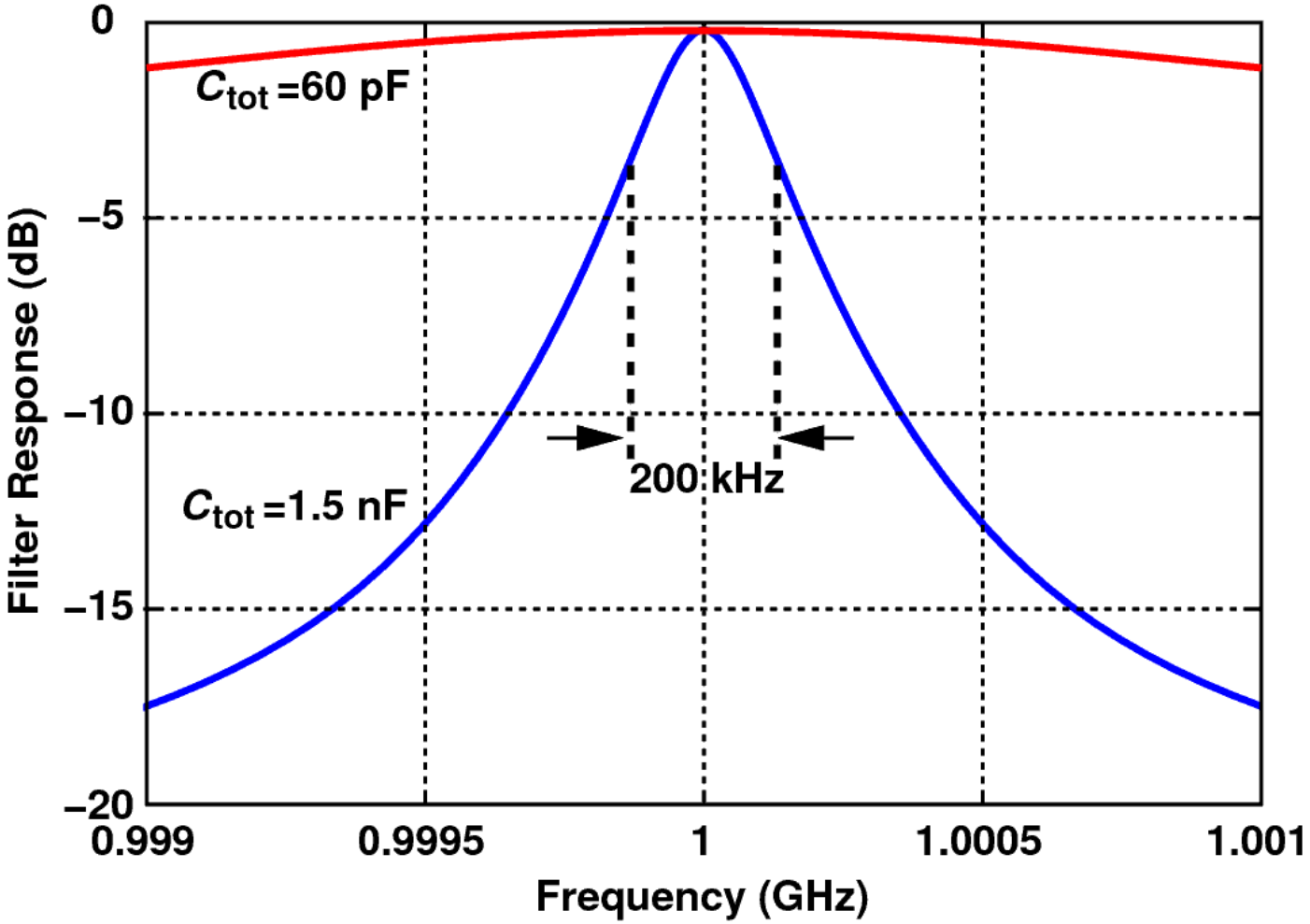
?

GSM

C_{tot} < 2 nF

P_{tot} ≤ 20 mW

But even larger caps are not enough …

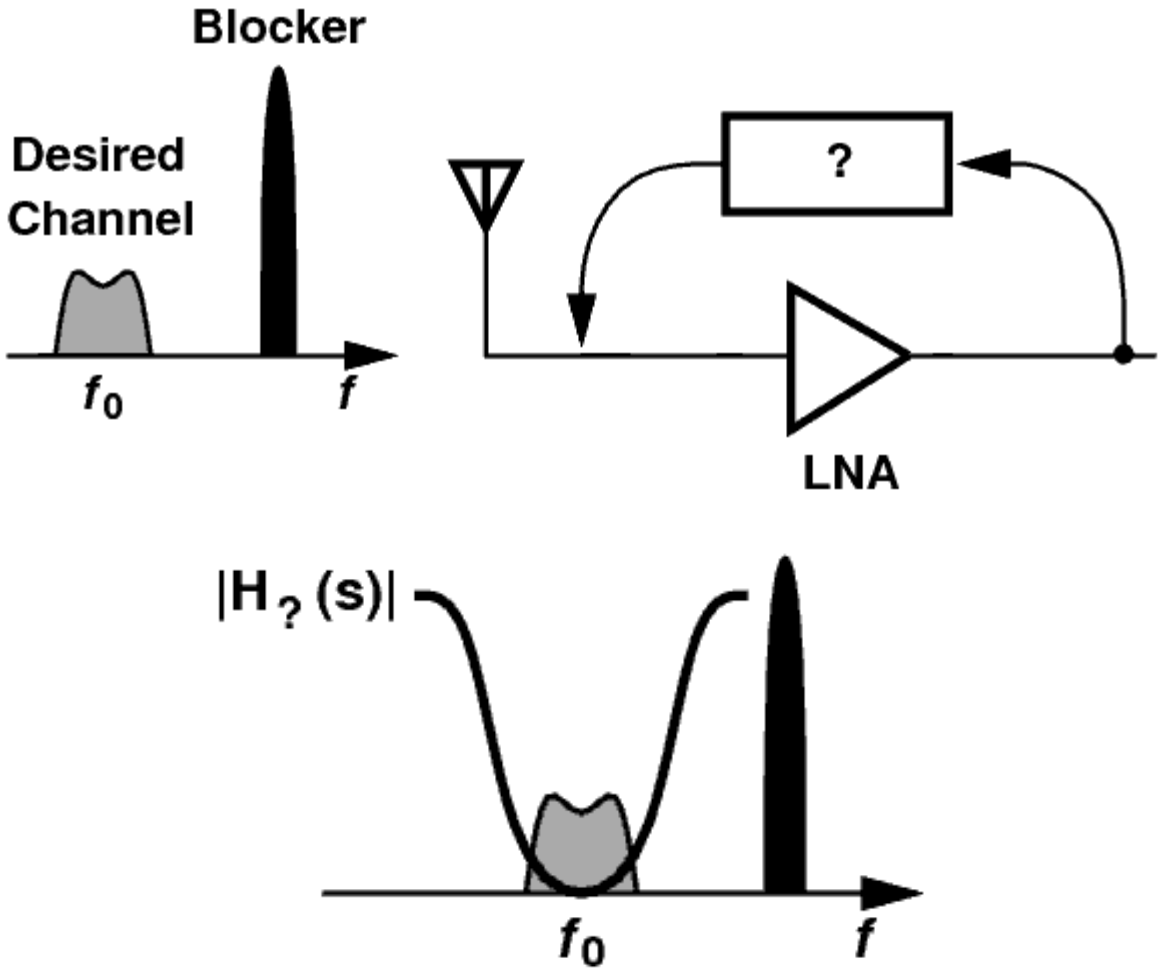


- First-order system → Not sufficiently selective

Preview of Proposed Concepts

- Miller Notch Filter
- Local Miller Notch Filter
- Unilateral Miller Notch Filter
- “Super Miller Effect”
- Polyphase Notch Filter

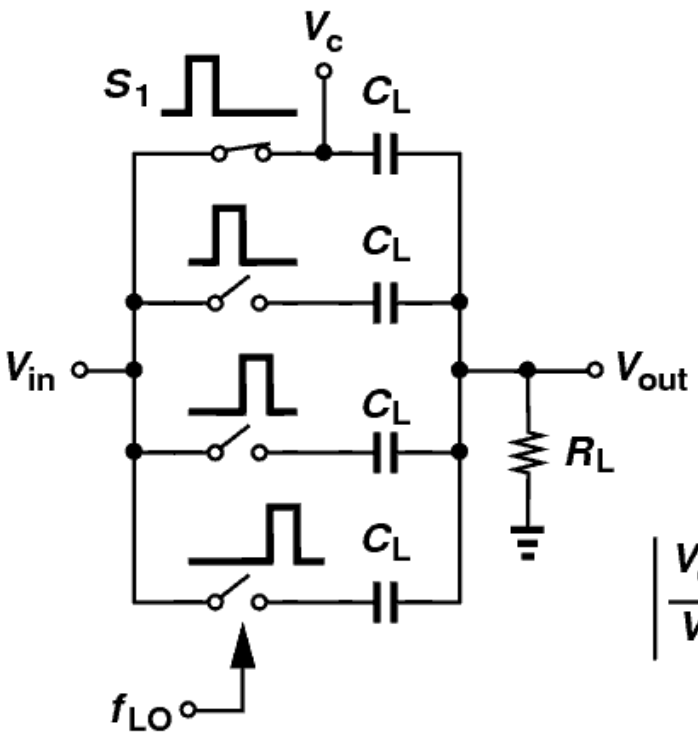
Can we filter at LNA input?

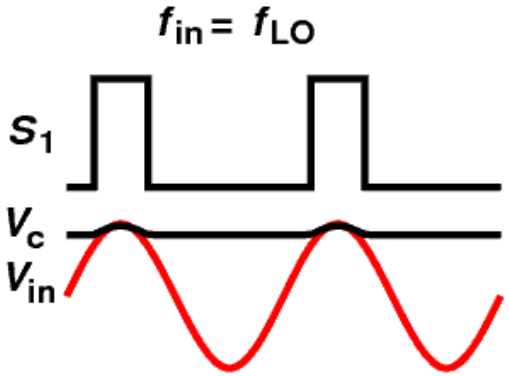


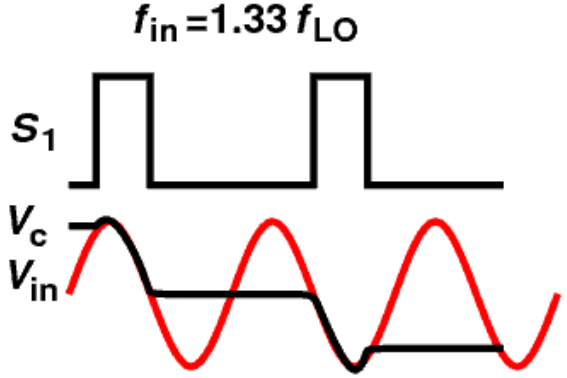
- **Notch filter must be accurate and programmable.**

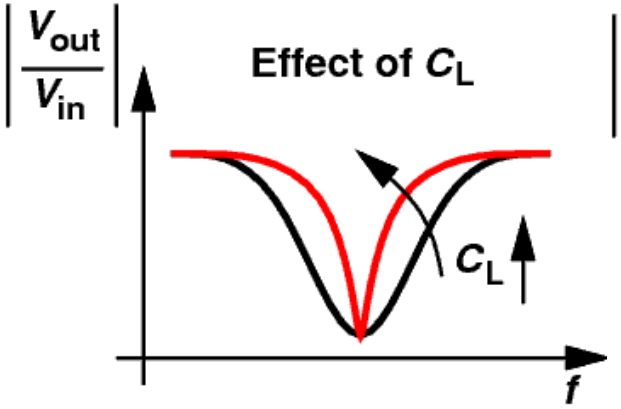
N-Path Notch Filter

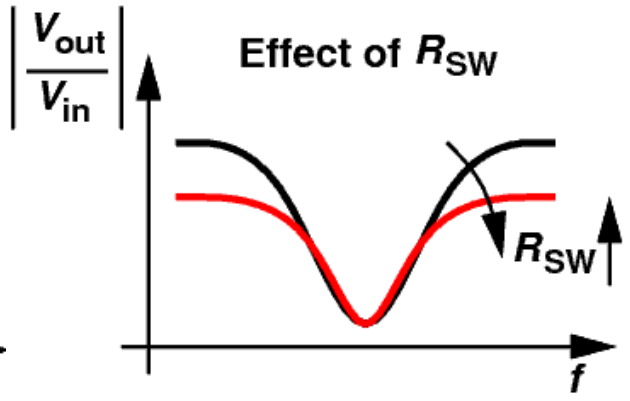
[M. A. Poole, U.S. Patent 3795877, 1974]
[A. Ghaffari, ISSCC, 2012]



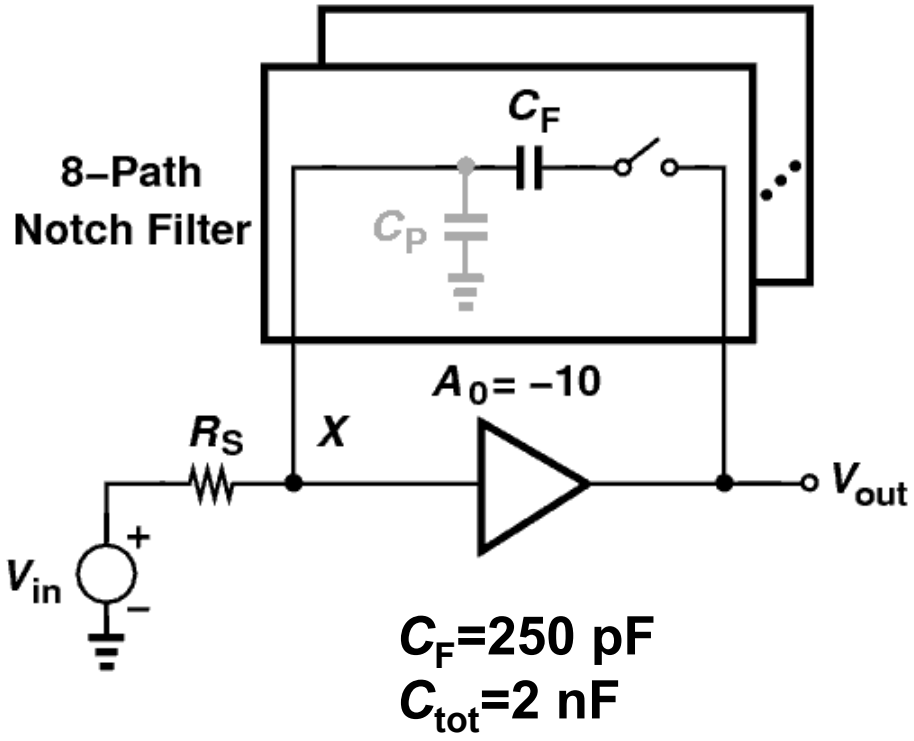




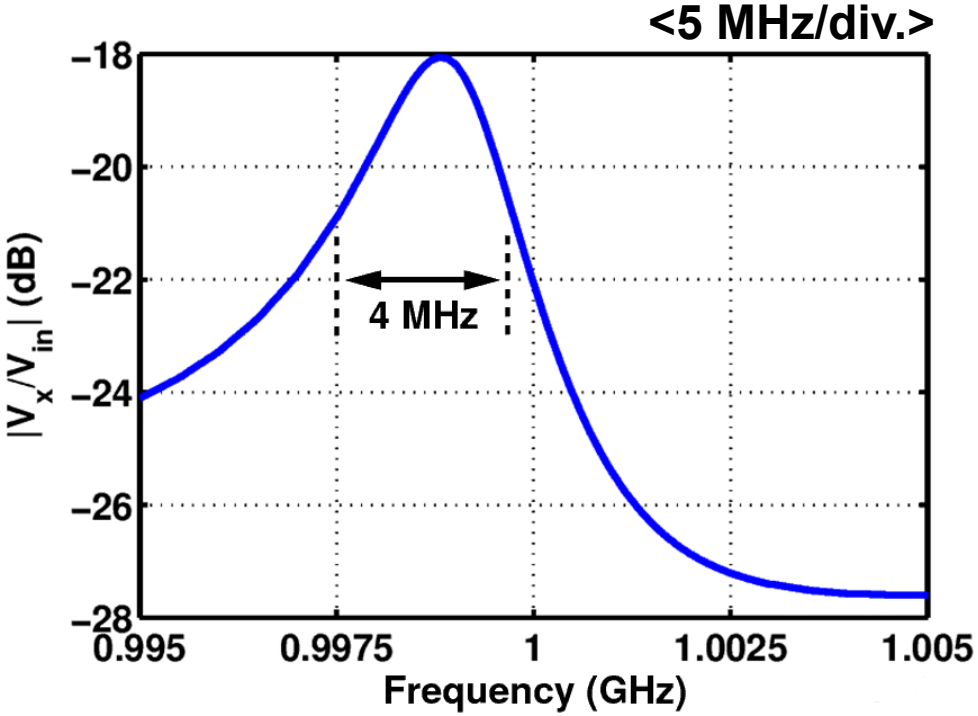




Proposed Idea #1: Miller Notch Filter

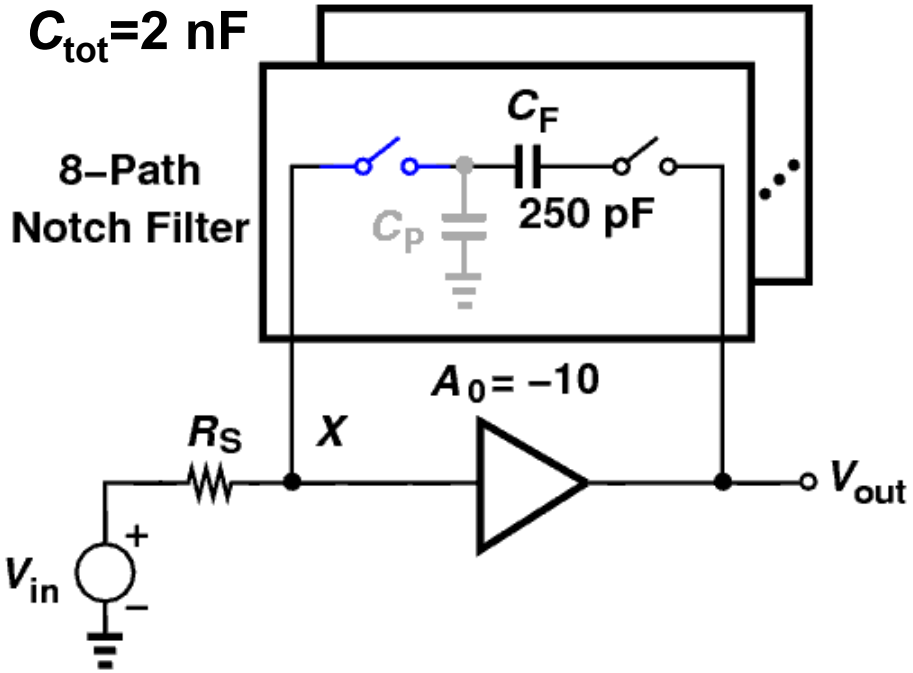


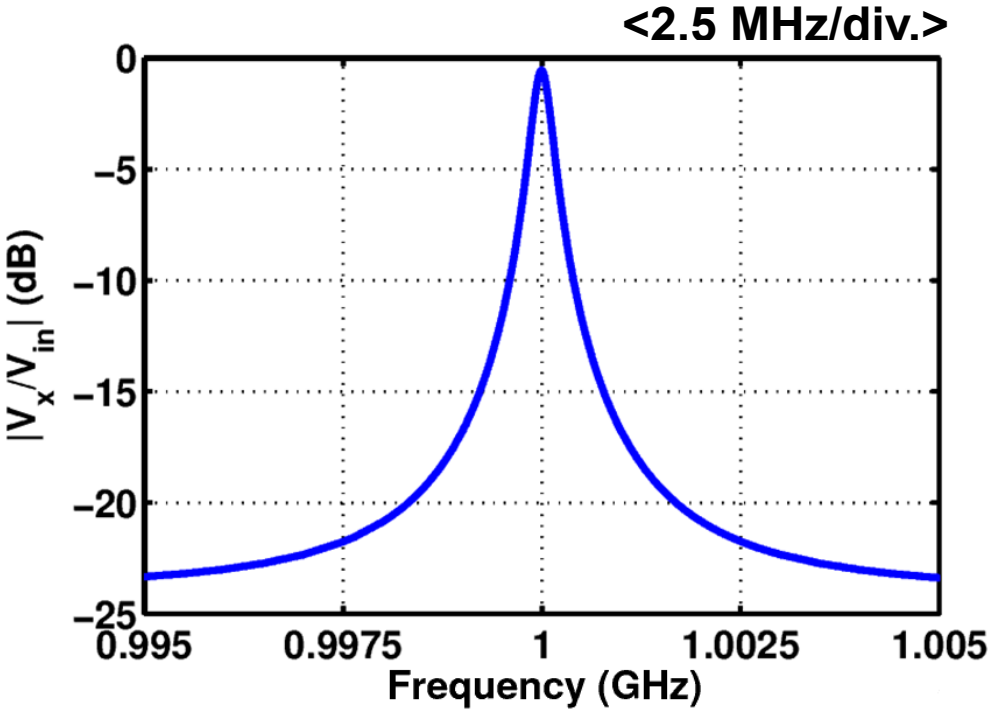
C_F=250 pF
C_{tot}=2 nF



- But C_P (~100 pF) loads the input.

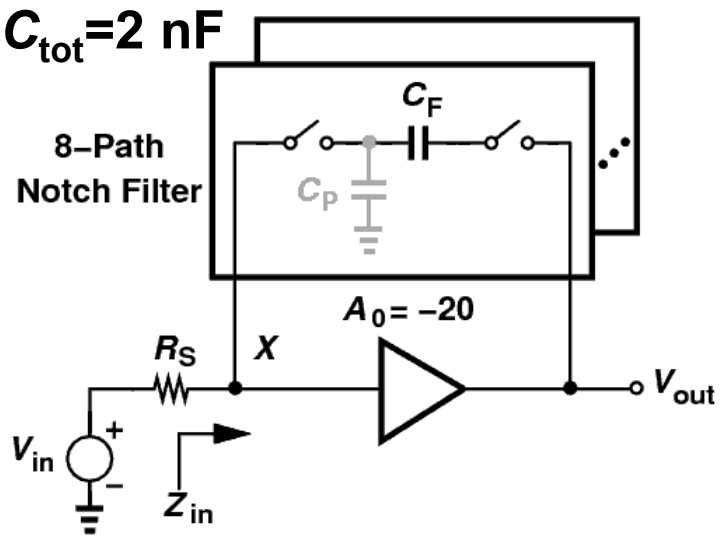
There's still hope: Dual-Switched Miller Notch Filter





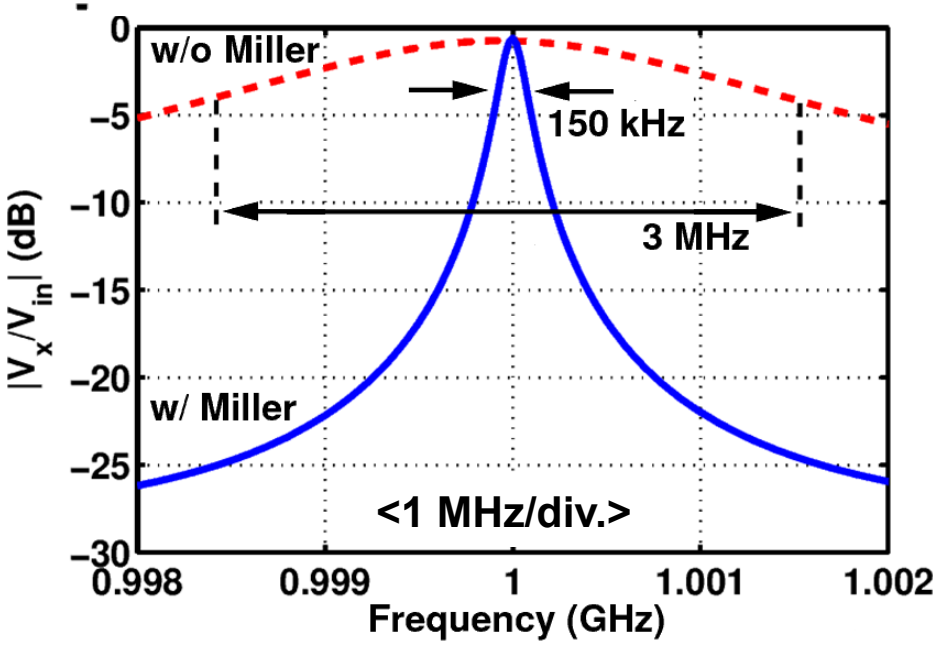
- C_P is upconverted to around f_{LO}.
- Narrow filter bandwidth can be achieved.

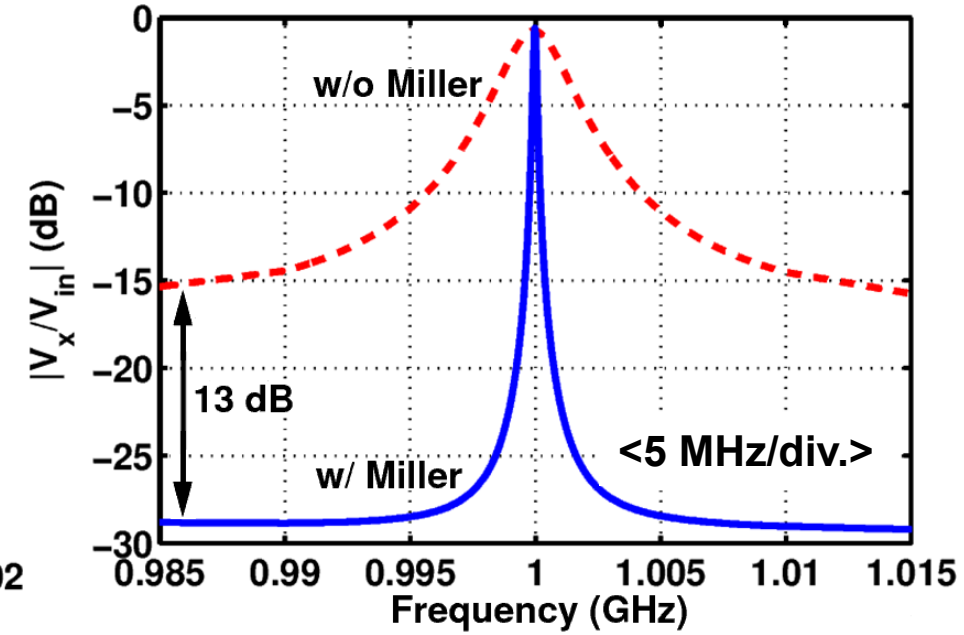
Advantages of Miller Notch Filter



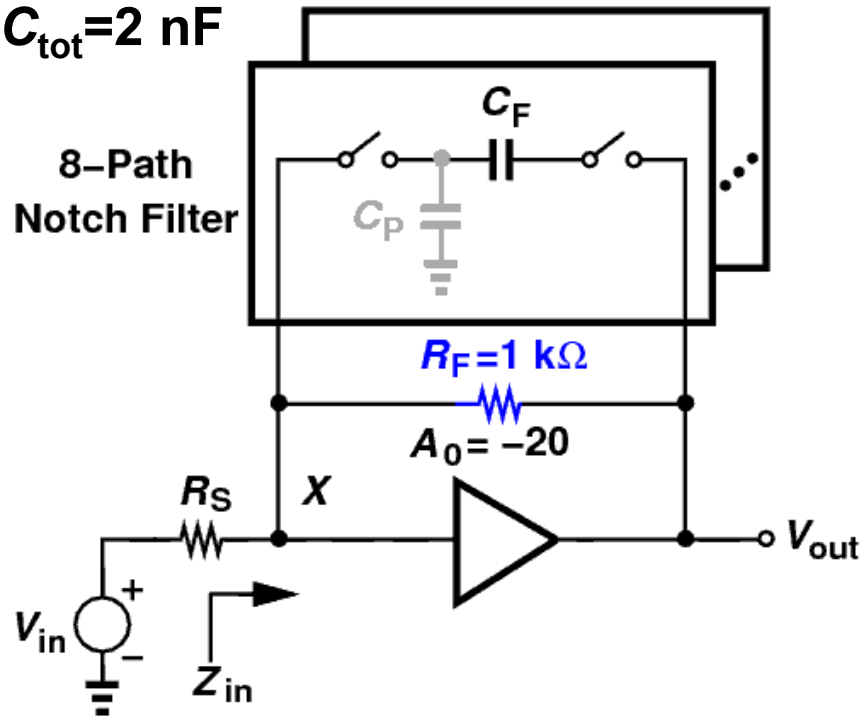
$$Z_{in}(\omega) = \frac{4R_{SW}}{1+A_0} + 8\sum_{n=-\infty}^{n=\infty} \frac{|a_n|^2}{j(1+A_0)C_F(\omega - n\omega_{LO})}$$

- Capacitance boosted by $1+A_0$
  → Easier to reach 200-kHz BW
- Switch resistance reduced by $1+A_0$
  → Less power in driving switches
- No amplifier in feedback → Stable



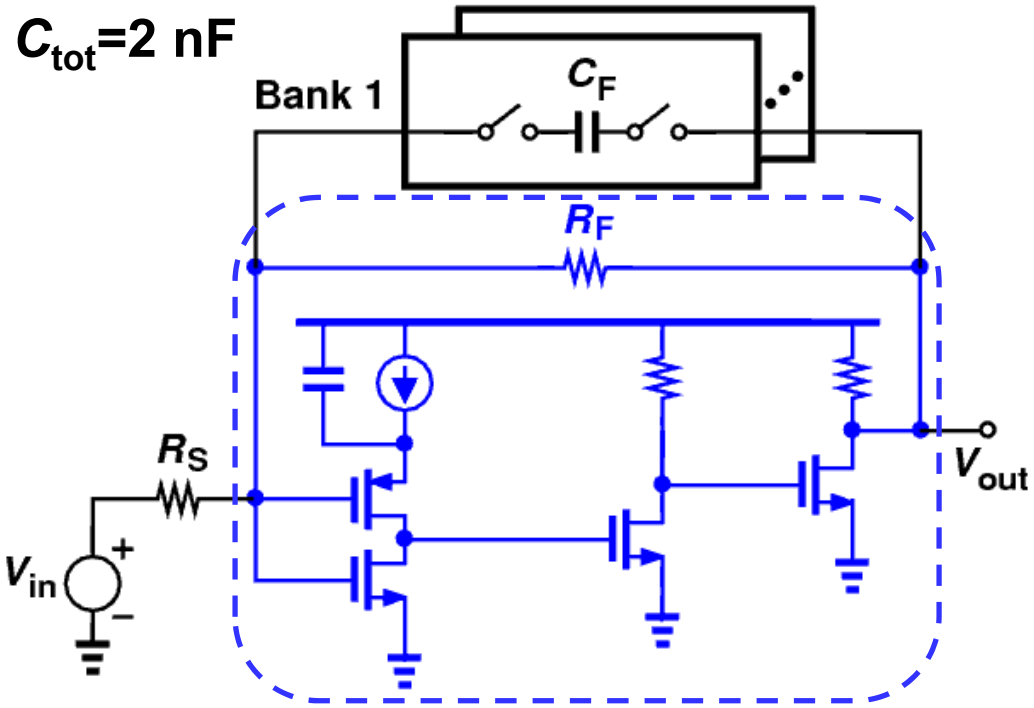


How about input matching?

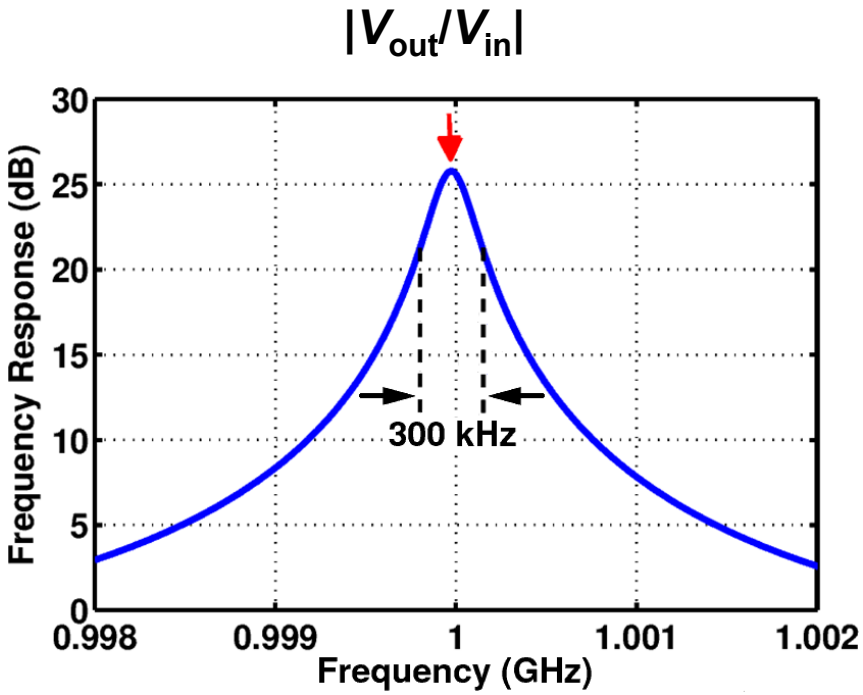


$$Z_{in}(\omega) = \frac{R_F}{1+A_0} \parallel \left[\frac{4R_{SW}}{1+A_0} + 8 \sum_{n=-\infty}^{n=\infty} \frac{|a_n|^2}{j(1+A_0) C_F (\omega - n\omega_{LO})} \right]$$

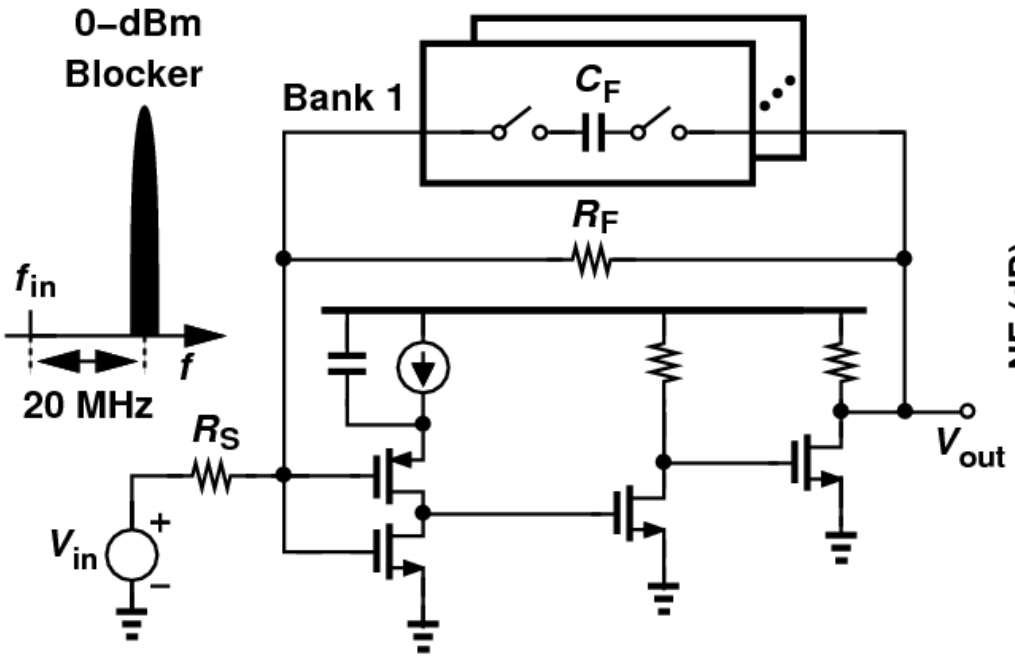
Front End with 8-Path Notch Filter

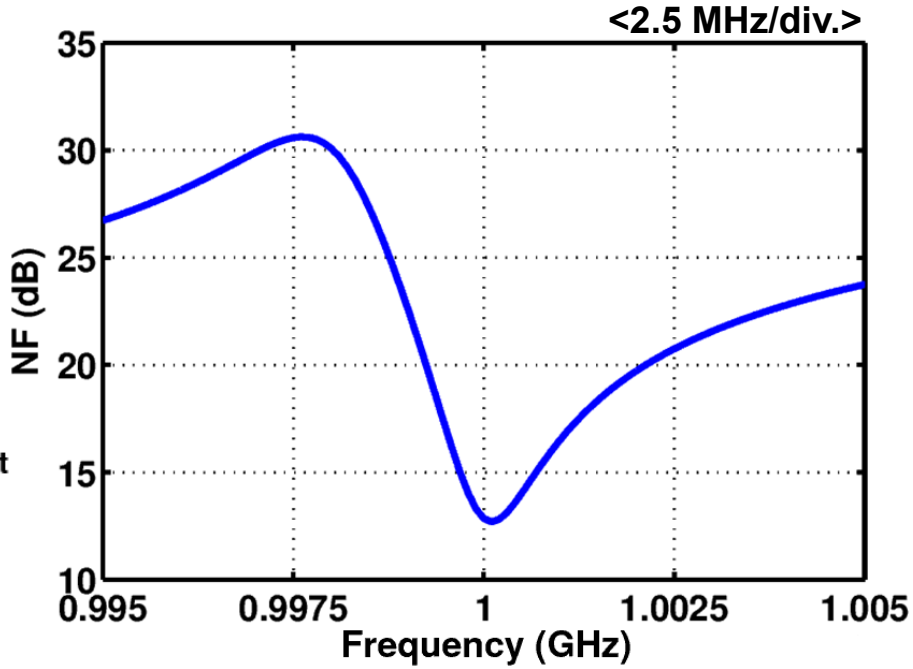


[Park and Razavi, JSSC, Apr. 2013]



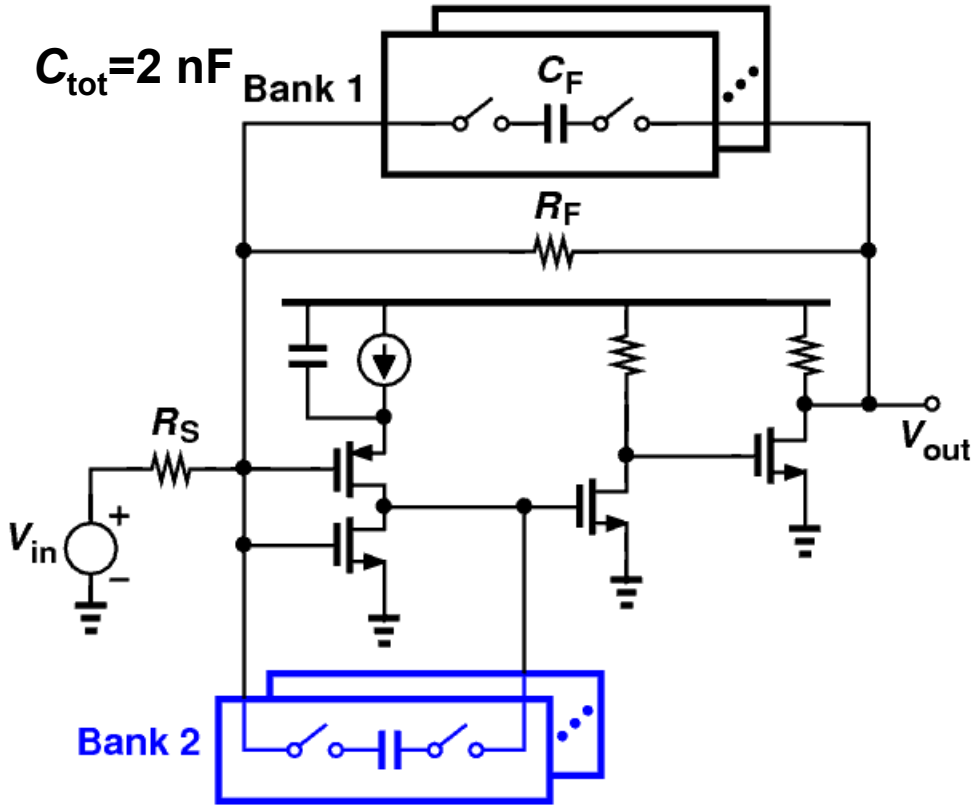
Quick Blocker Test

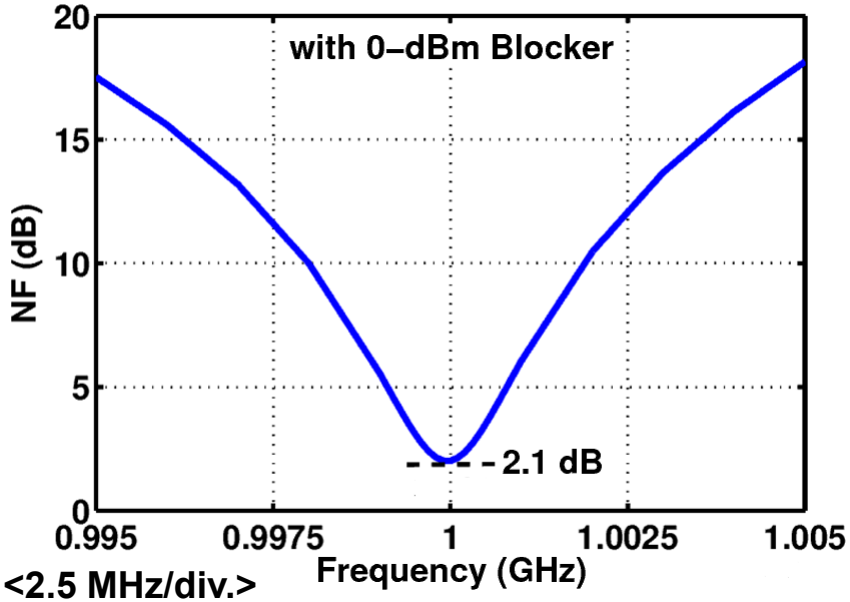


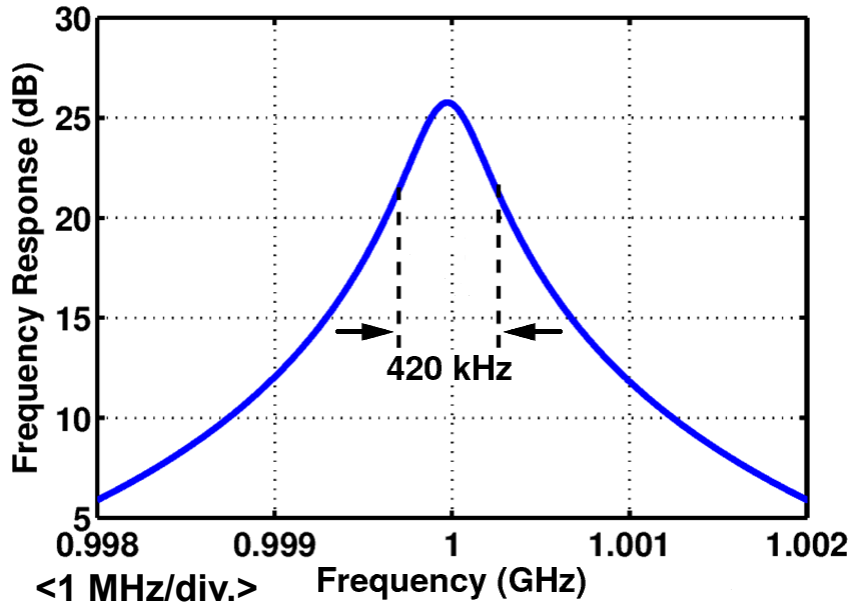


- **0-dBm blocker saturates second and third stages. (LNA core P_{1dB}= -25 dBm)**

Proposed Idea #2: Local Miller Notch Filter

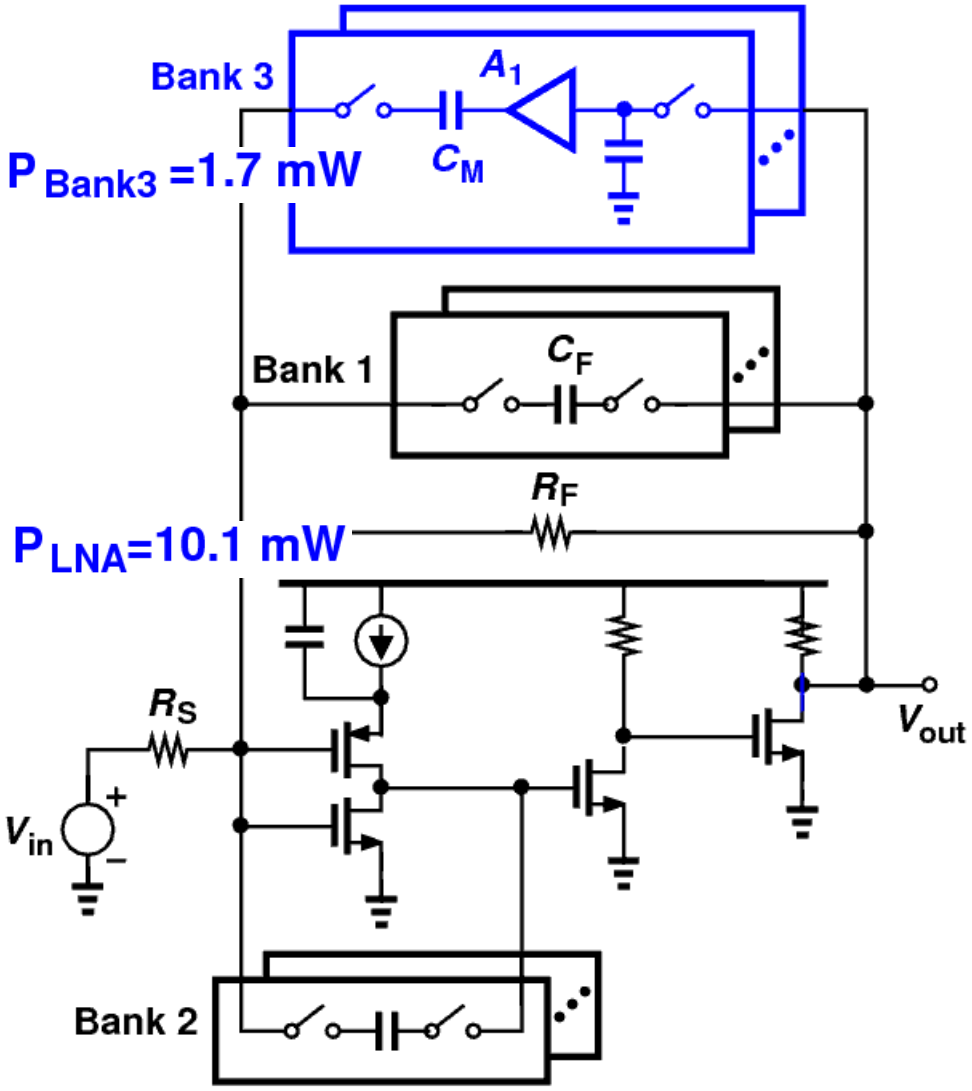


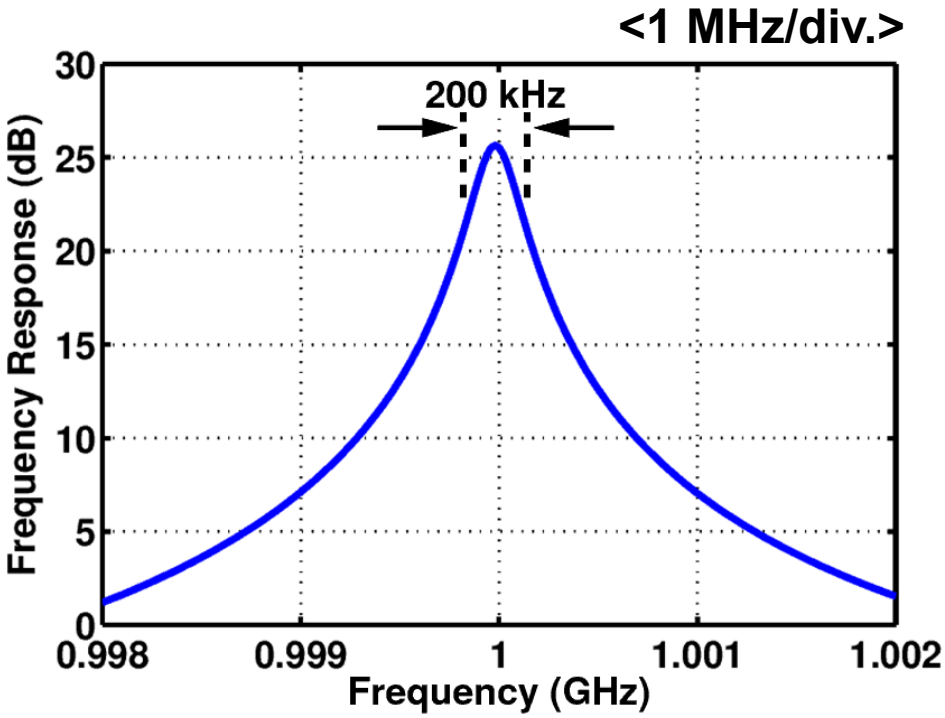




- Bank 2 helps suppress 0-dBm blocker.
- But,
  - Bandwidth has increased.
  - Still first order

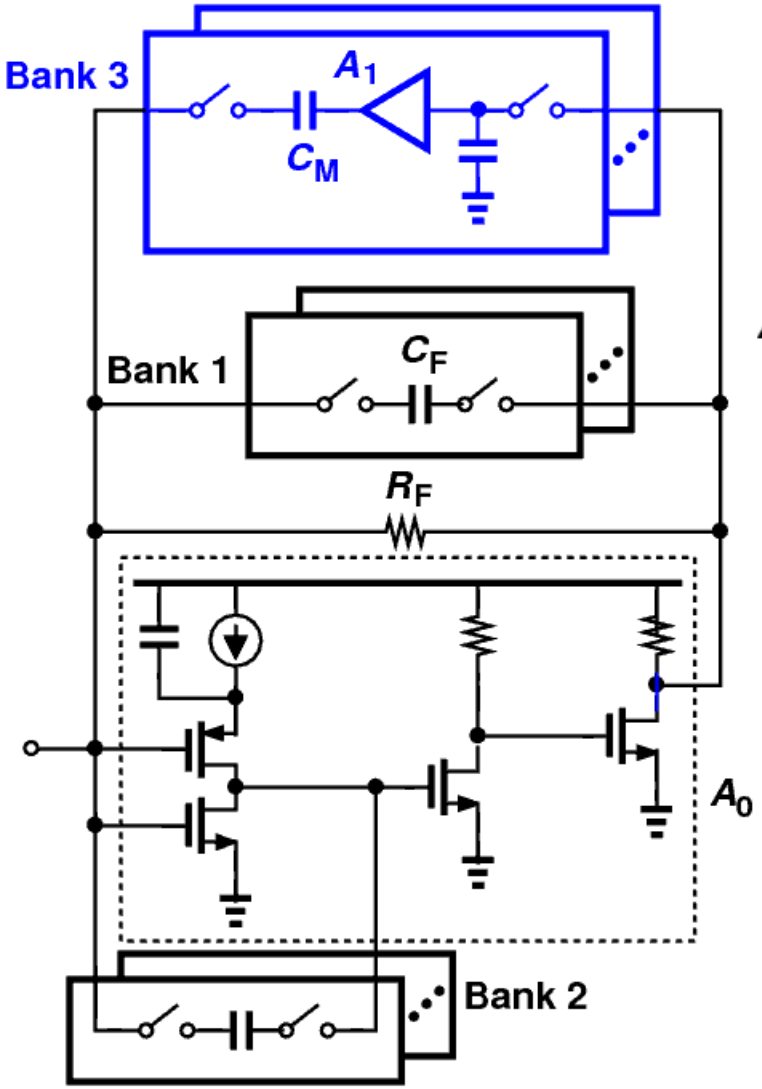
Proposed Idea #3: Unilateral Miller Notch Filter





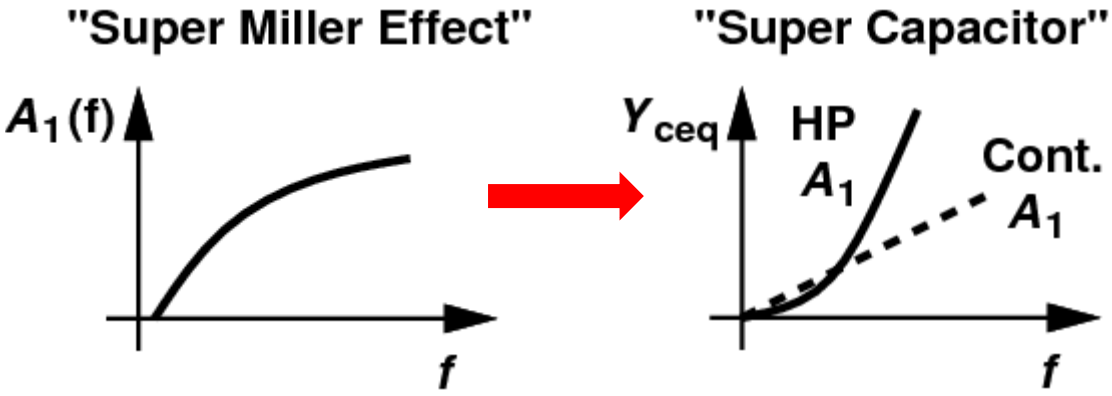
- A_1 "amplifies" Miller effect
  → 200-kHz BW with 10 pF
  → C_{tot}= 1.3 nF
- But how about stability?
- Still first order

Proposed Idea #4: "Super Miller Effect"

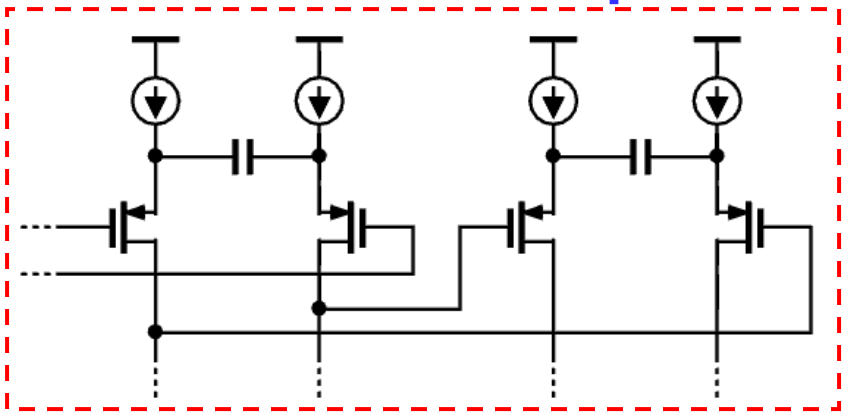


$$C_{eq} = C_M\left(1 + A_0 A_1\right)$$

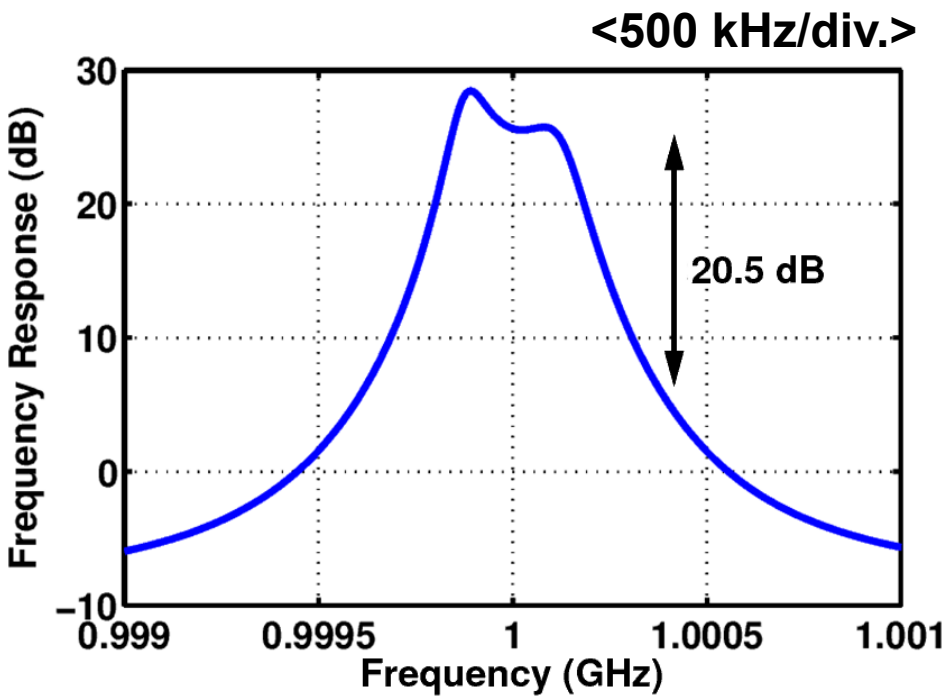
- Shape the frequency response of A_1.

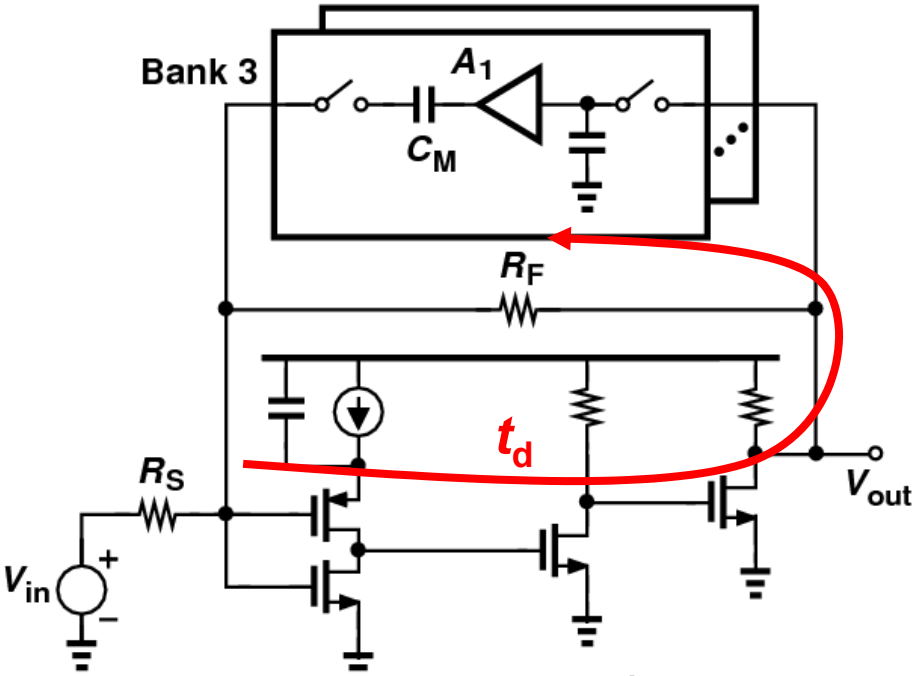


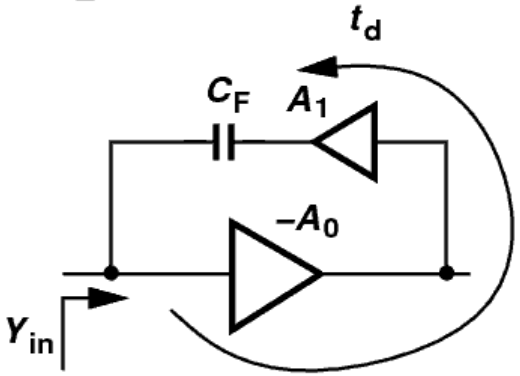
- Two zeros for sharp selectivity



But all is not well …





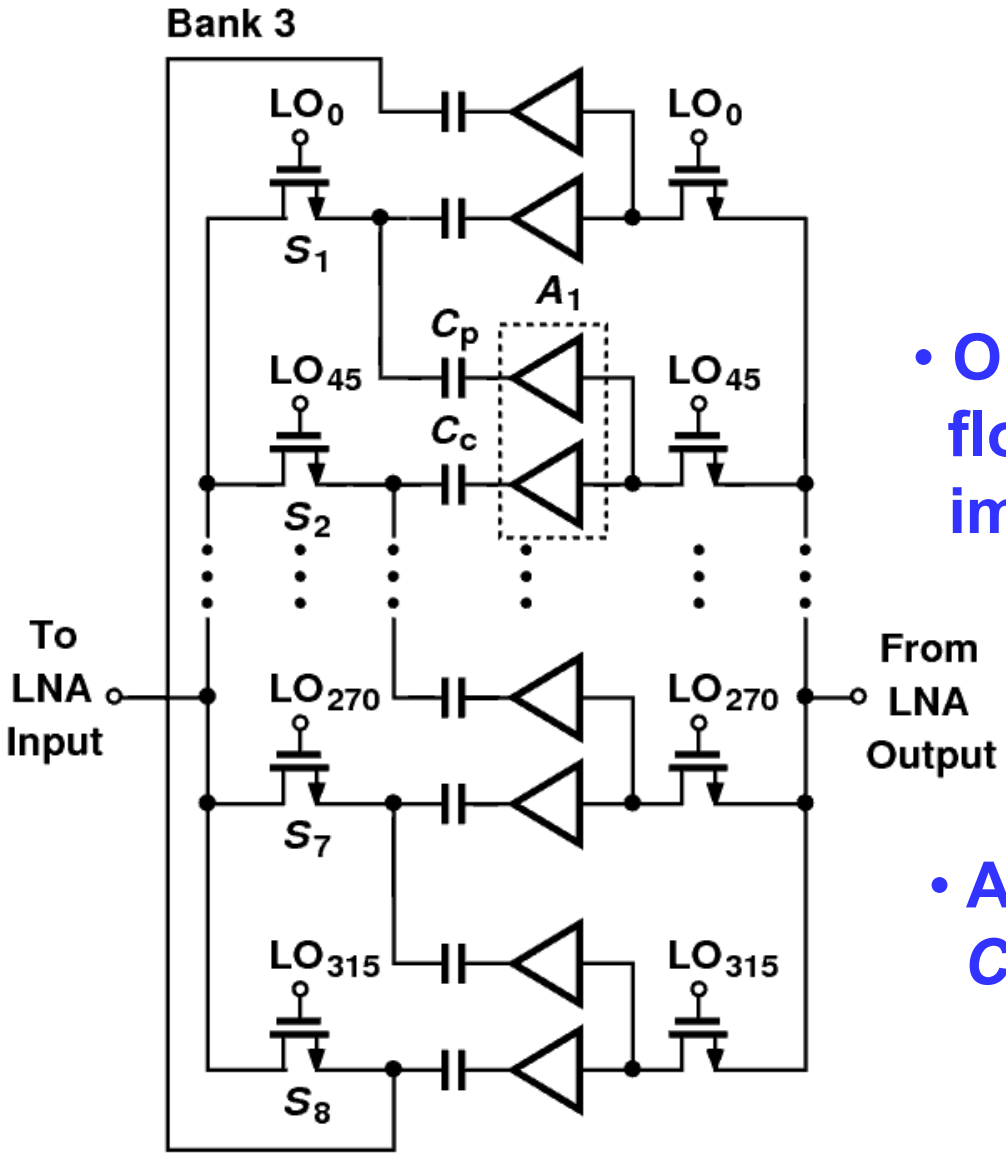


- 20.5-dB rejection at 400-kHz offset (center of next adjacent channel)
- C_{tot}=1.76 nF

- But, we have 4 dB of peaking.

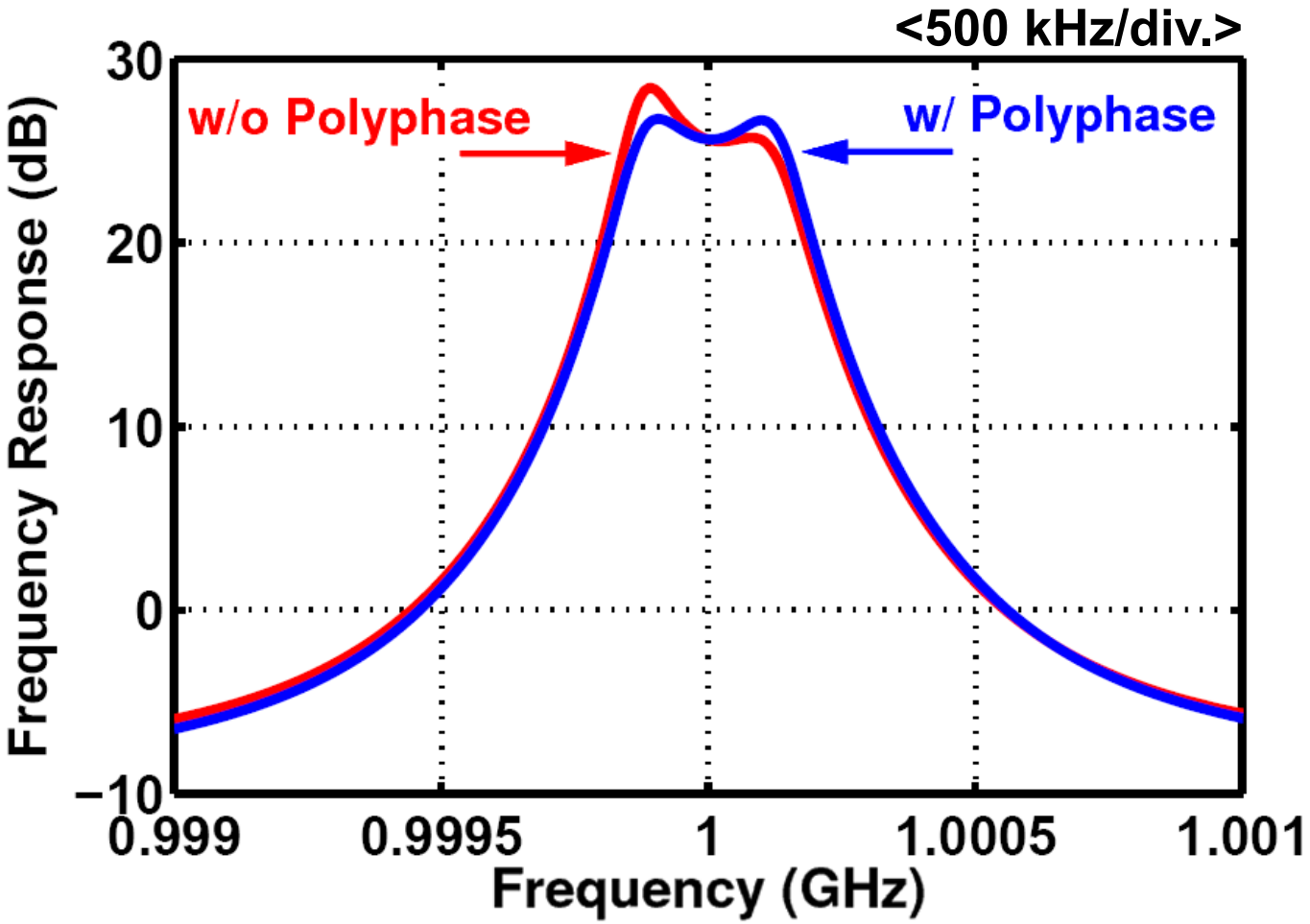
$$Y_{in} = j2\pi f \left(1 + A_0 A_1 e^{-j2\pi f t_d}\right) C_F$$

Proposed Idea #5: Polyphase Notch Filter



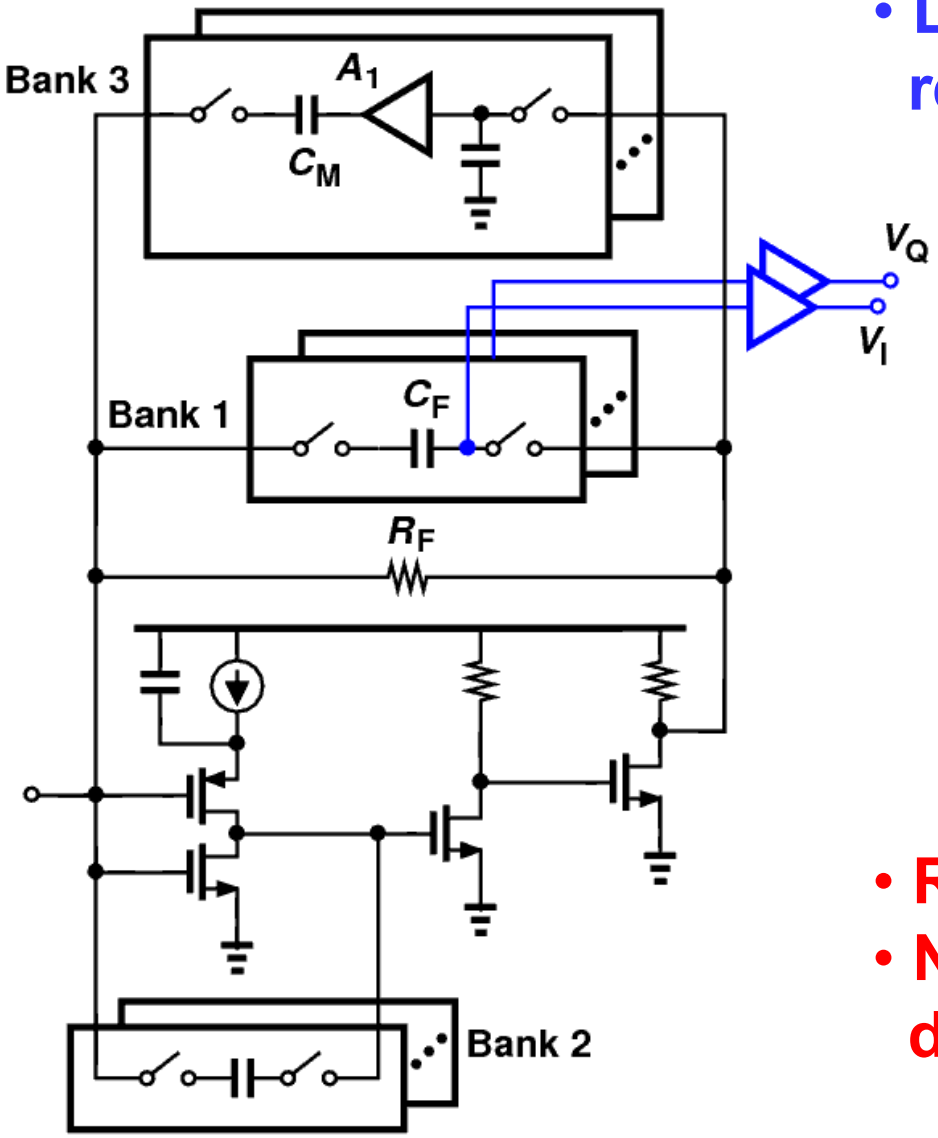
- Objective: Make the current flowing through S_1-S_8 imaginary.
- Achieved by proper choice of C_C/C_P ratio.

Now all is well …

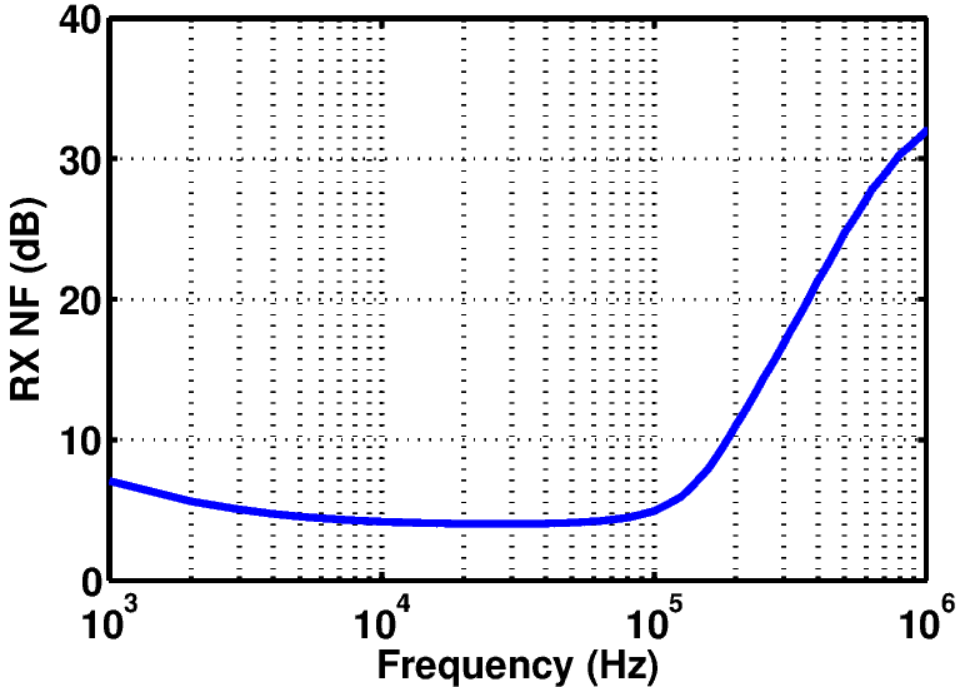


- Properly chosen C_C/C_P corrects the center frequency.
- 3-dB bandwidth unaffected

Towards a Complete Receiver

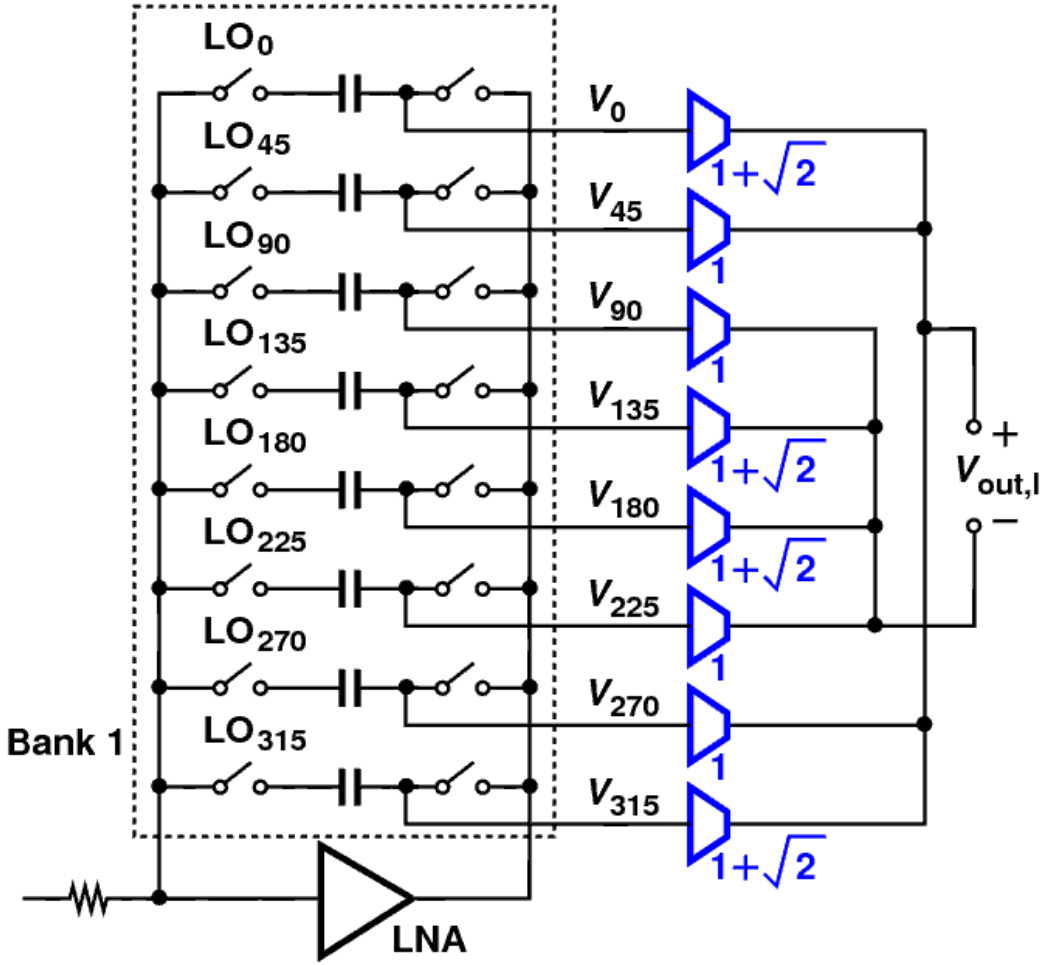


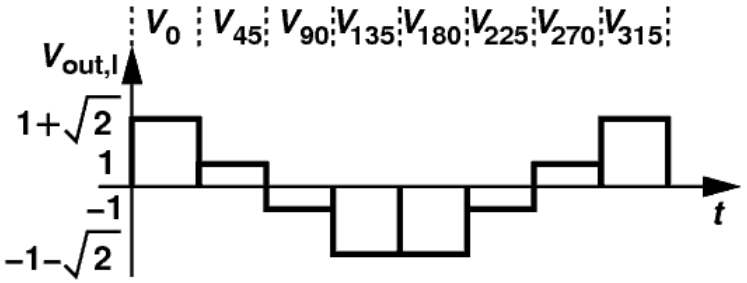
- Linearity of BB amps is greatly relaxed.



- RX NF at 50 kHz=4 dB
- Noise at LO harmonics downconverted to baseband

How to Reject Noise at LO Harmonics



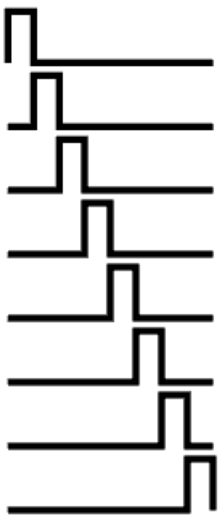


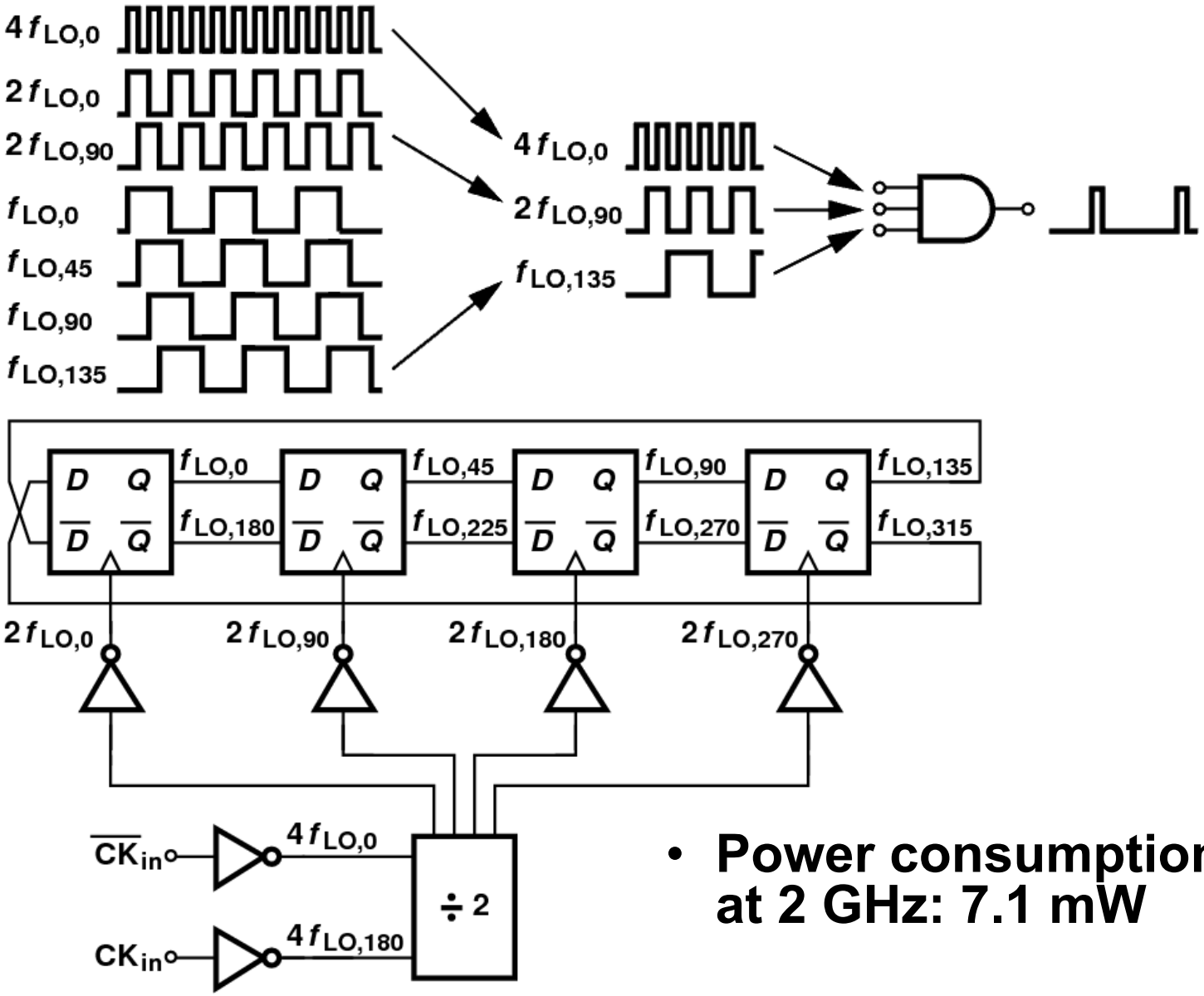
- Harmonic rejection at 3rd, 5th, 11th, 13th, …

- How about noise & power of baseband amplifiers?
  - NF contribution: 0.4 dB at 50 kHz.
  - Total Power: 1.1 mW

Low-Power Multi-Phase LO Generation

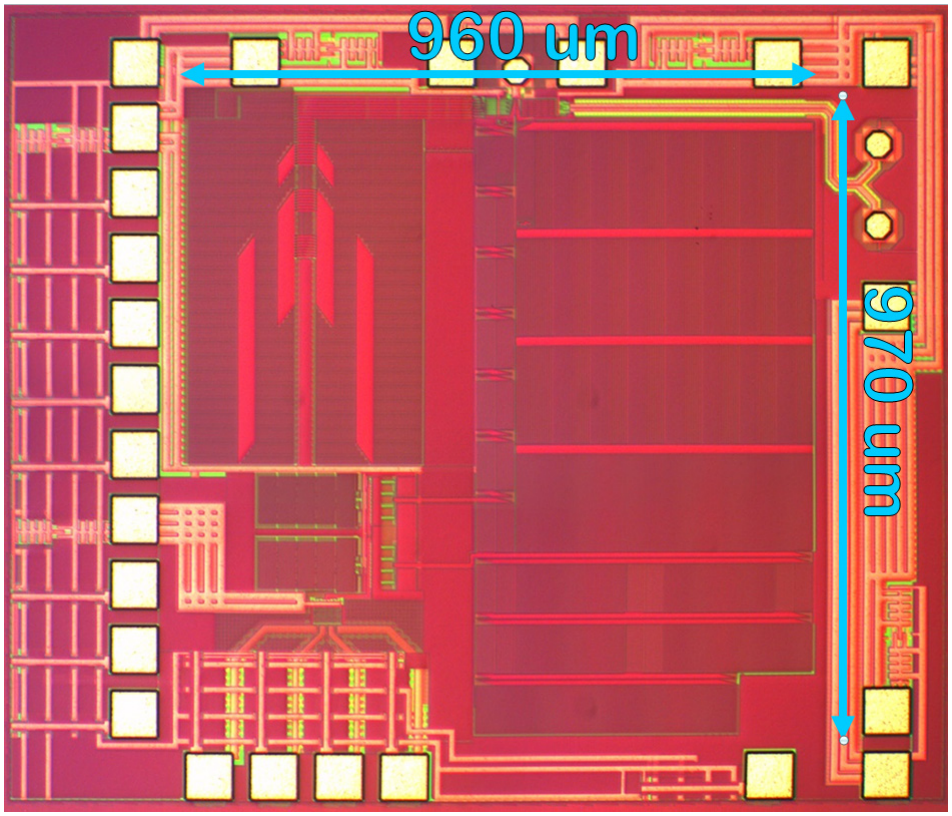
- **Need 8 phases:**





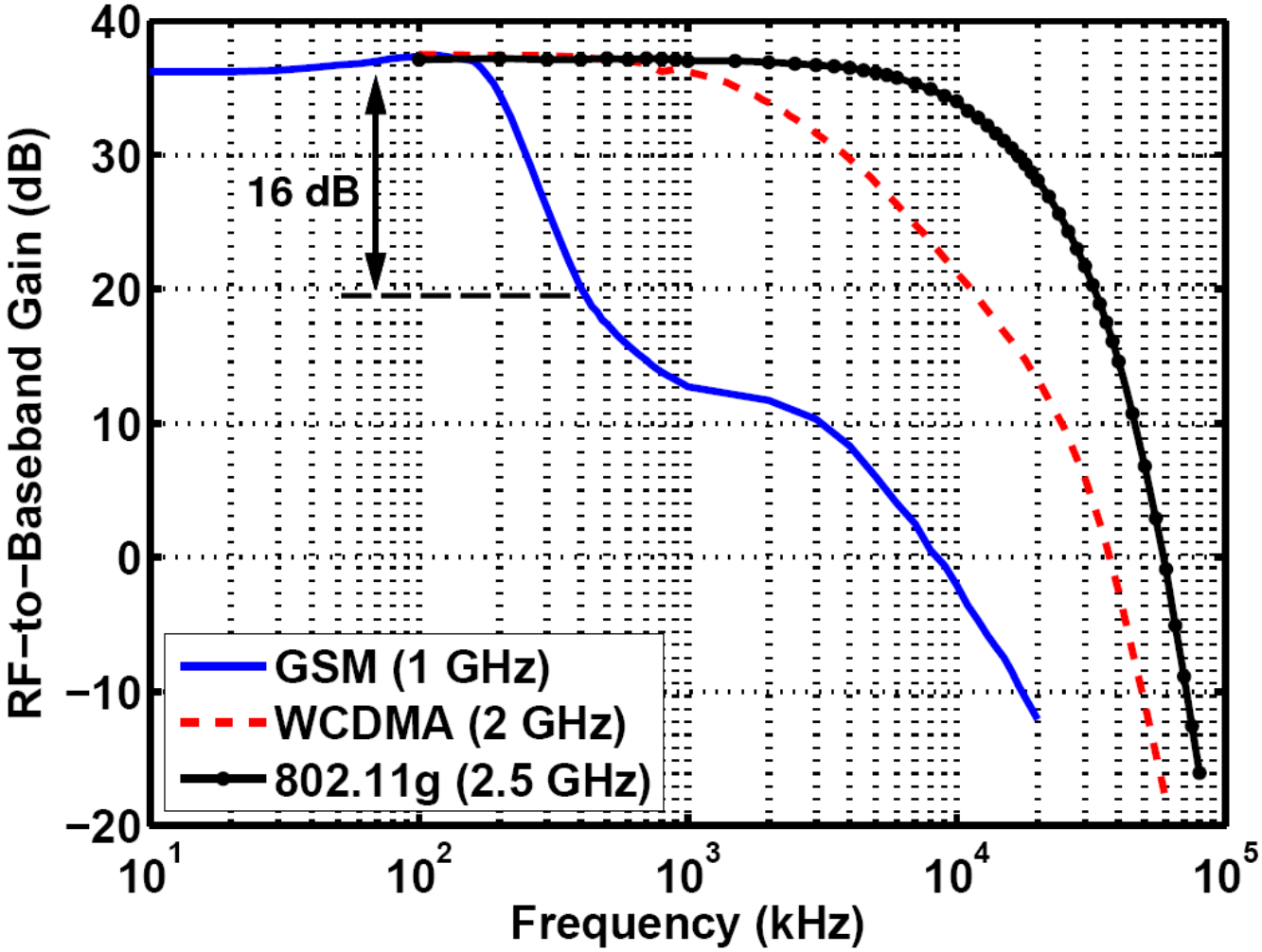
- **Power consumption at 2 GHz: 7.1 mW**

Receiver Die Photograph



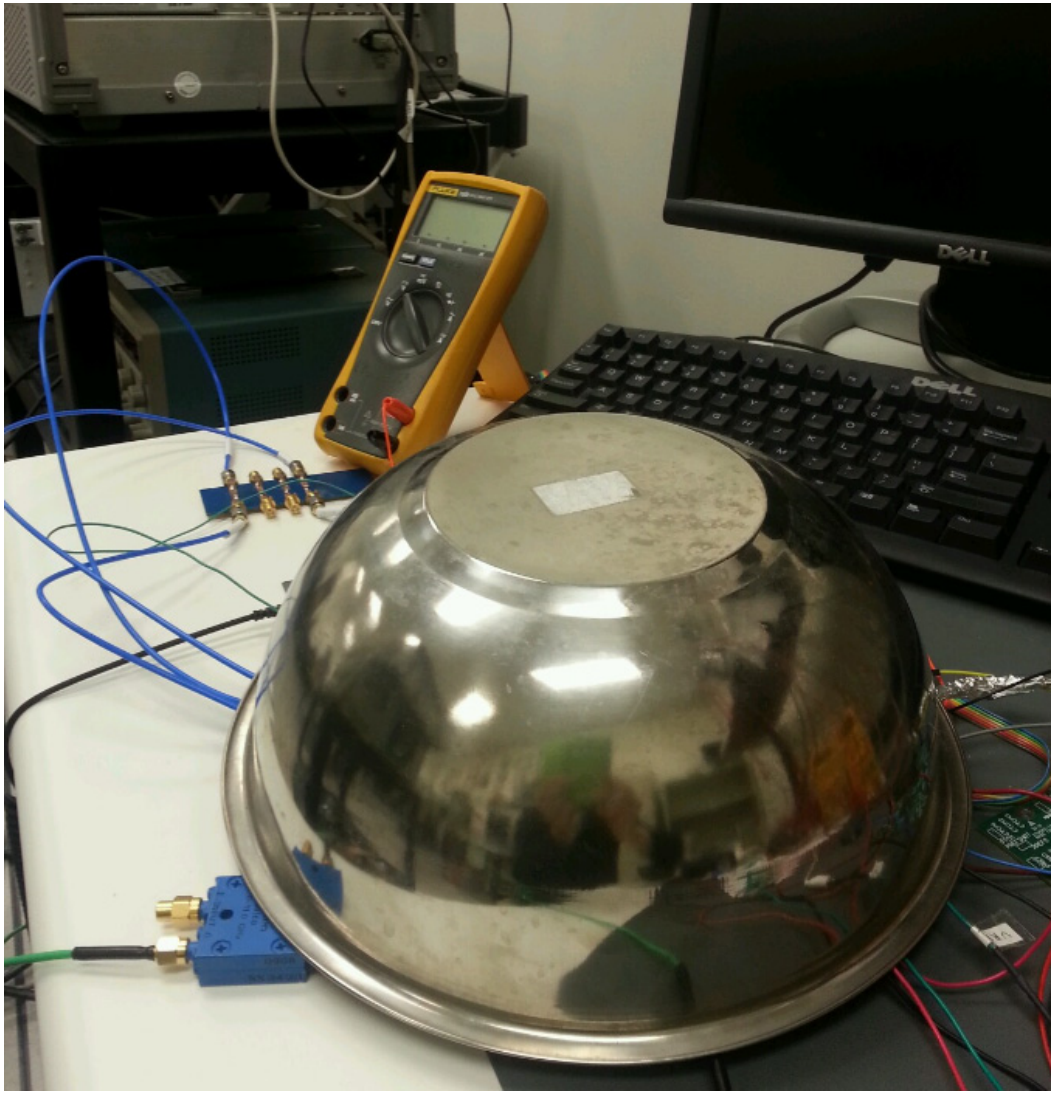
- Supports GSM, WCDMA, 802.11b/g.
- Power Dissipation: 20 mW
  - LNA Core: 10.1 mW
  - Bank 3 Amps: 1.7 mW
  - Baseband Amps: 1.1 mW
  - LO Gen.: 7.1 mW

Measured RF to Baseband Gain

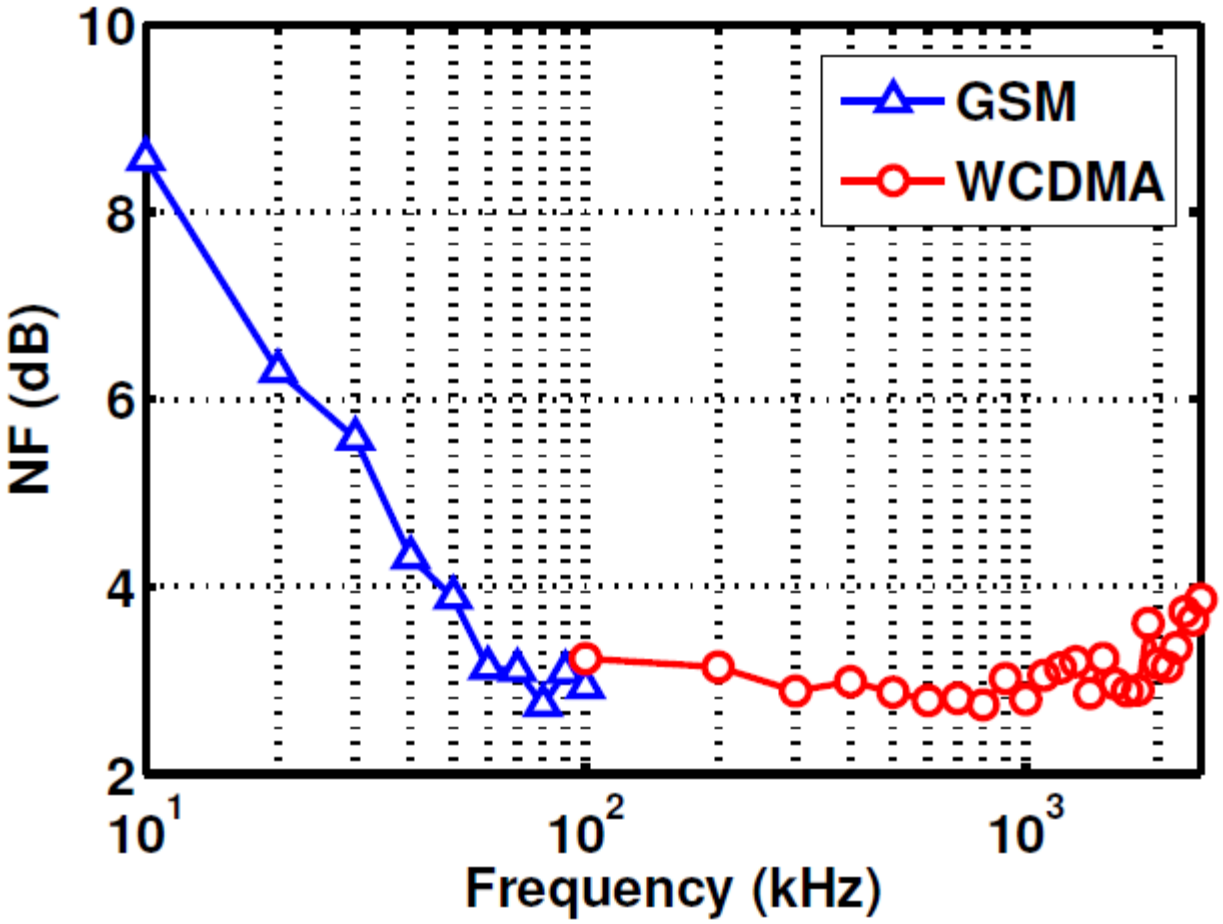


- Variable 3-dB RF channel bandwidth from 350 kHz to 20 MHz

Test Setup for NF Measurement

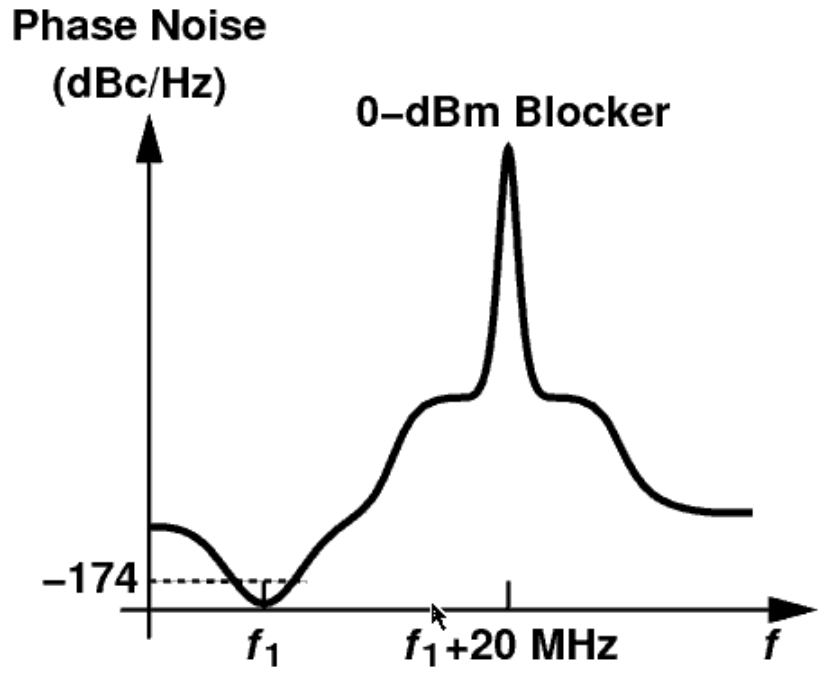


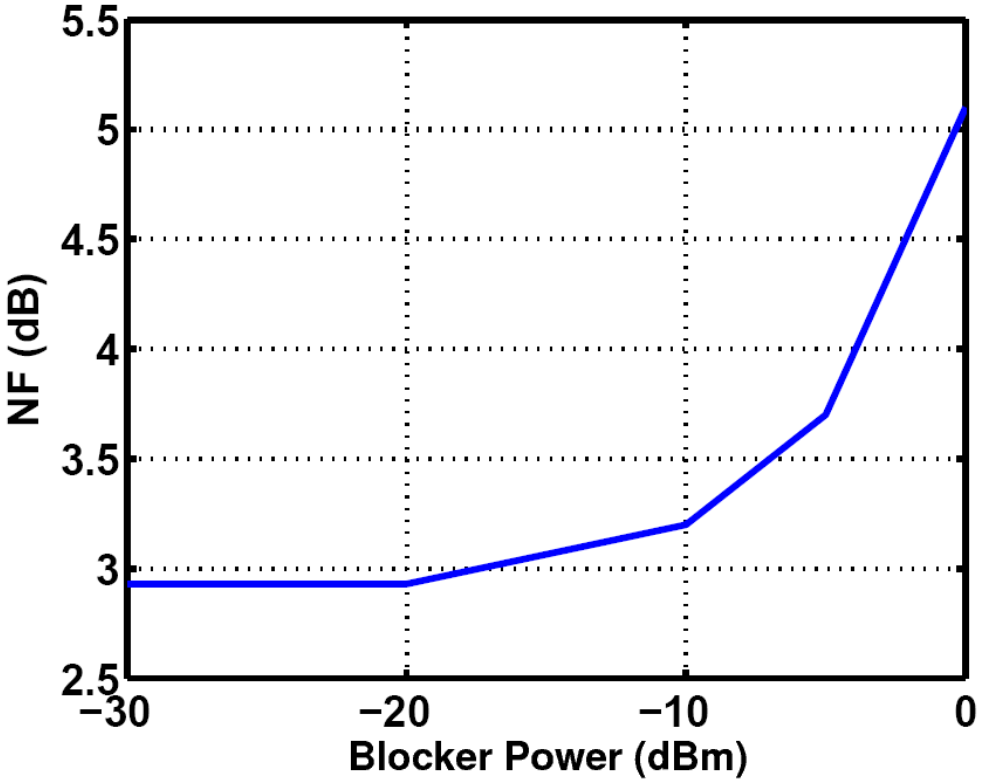
Measured RX Noise Figure

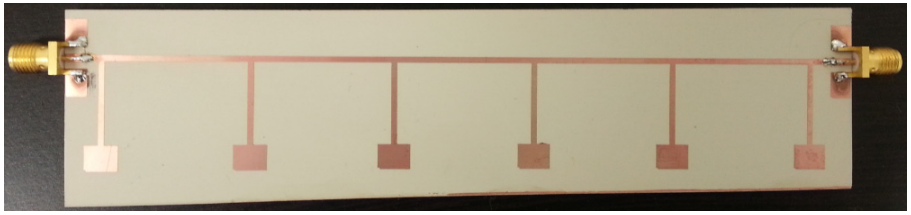


- Flicker noise at low frequencies mostly due to LO source.
- 2.9-dB NF at 100 kHz.

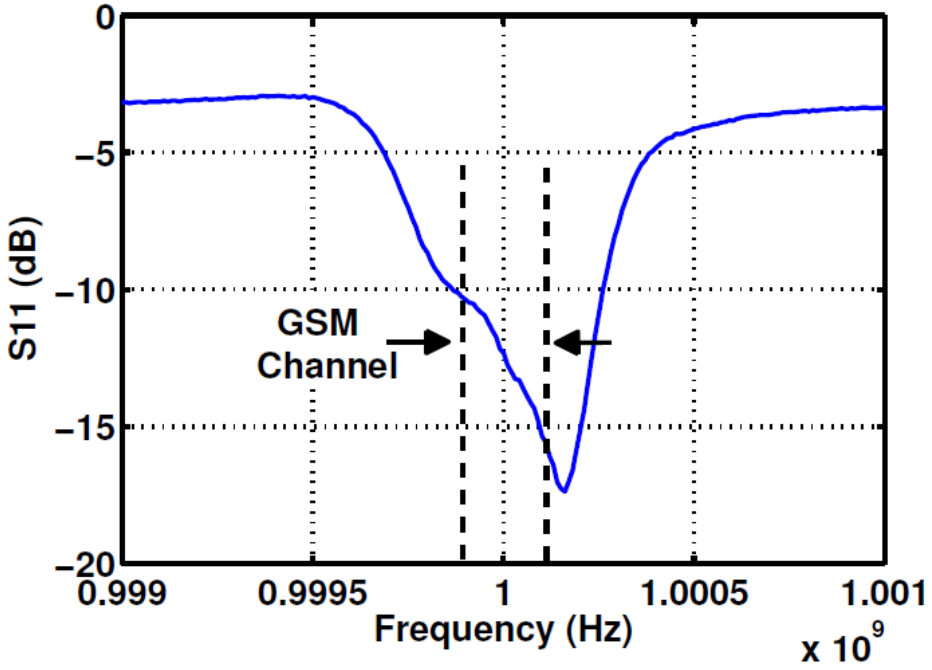
Measured NF with 0-dBm Blocker

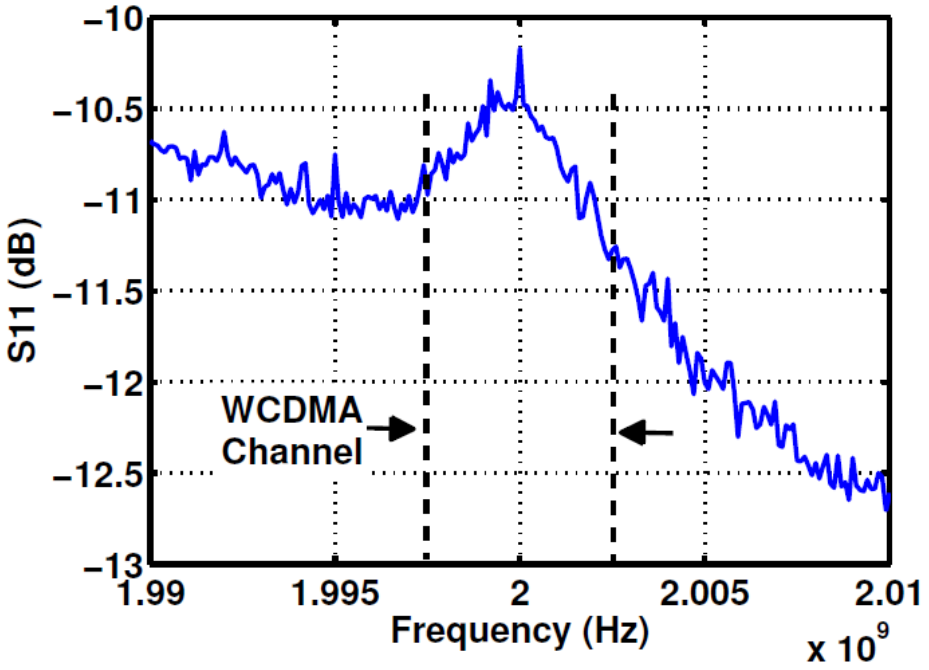






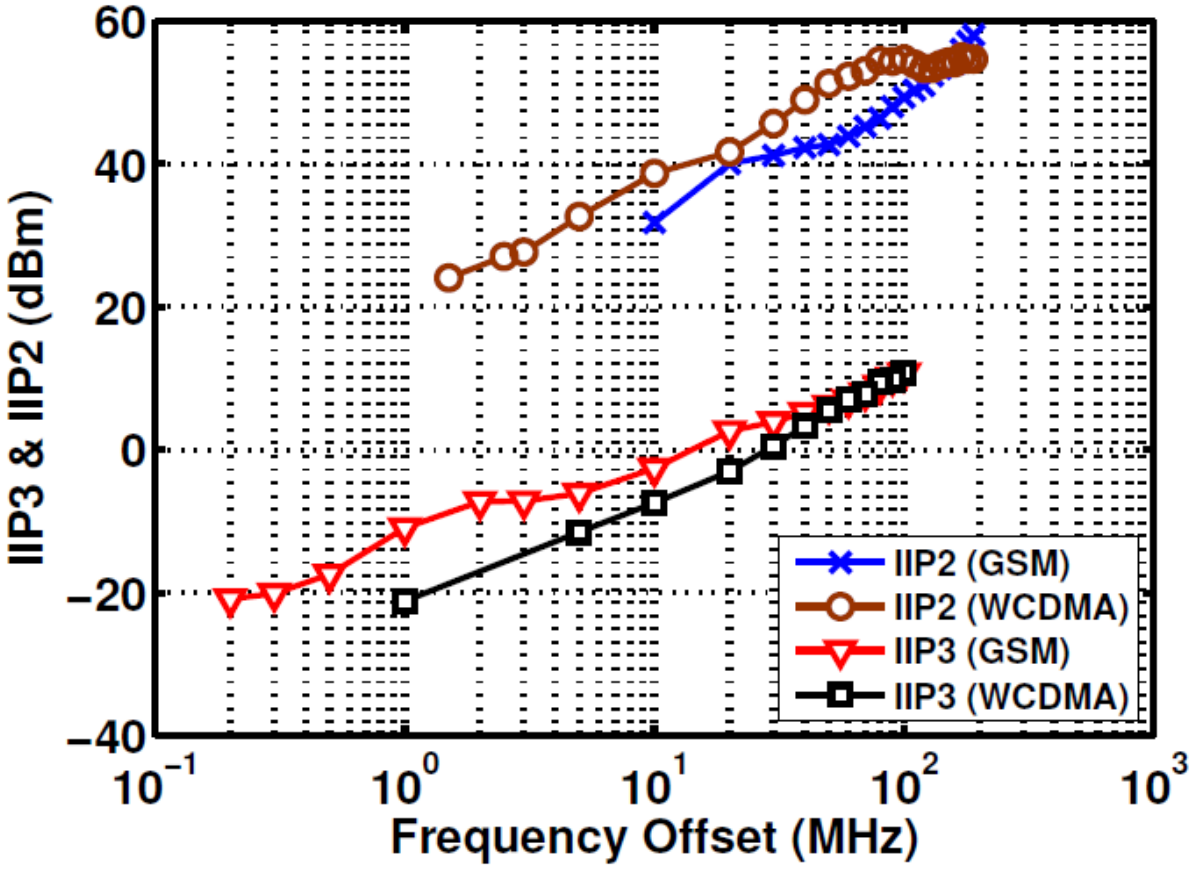
Measured S_{11} for GSM/WCDMA





- $|S_{11}| < -10$ dB across desired channel

Measured IIP_2 and IIP_3



Performance Comparison

	Murphy ISSCC 2012	Youssef ISSCC 2012	Fabiano ISSCC 2013	This work
Input Frequency [MHz]	80 ~ 2700	1000 ~ 2500	1800 ~ 2400	50 ~ 2500
Channel Bandwidth [MHz]	N/A	5	N/A	0.35 ~ 20
Gain [dB]	72	30	45.5	38
NF [dB]	1.9	7.6	3.8	2.9
NF with 0–dBm Blocker [dB] (at Given Offset)	4.1 (80 MHz)	N/A	7.9 (20 MHz)	5.1 (20 MHz)
Out–of–Band–IIP3 [dBm]	13.5	12	18	10
LO Leakage to Antenna [dBm] @ 2 GHz	–65	N/A	N/A	–67
Active Area [mm^2]	1.2	< 0.06	0.84	0.82
Supply Voltage [V]	1.3	1.2	1.2/1.8	1.2
Power Consumption [mW]	65 (2 GHz)	62[1]	35[2] (2 GHz)	20 (2 GHz)
CMOS Technology	40 nm	65 nm	40 nm	65 nm

[1] Excluding clock circuitry [2] With a 1.8 V supply for LO divider

Conclusion

- A multitude of new circuit techniques have been presented:
  - Miller Notch Filter
    → Significant Cap. and LO Power Reduction
  - Unilateral Miller Notch Filter
    → Further Magnified Miller Effect
  - "Super" Miller Effect
    → High-Order BPF
  - Polyphase Notch Filter
    → Removes peaking in response
  - Low-Power Multi-Phase LO Generation
- A 20-mW receiver compliant with GSM/WCDMA noise figure, selectivity, and blocking is reported.

Acknowledgment

- Lincoln Lab. and Realtek for research support

- TSMC for chip fabrication